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High Frequency Properties of the Geonium Chip Penning Trap and Development of a Broadband Ion Detection System

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Declaration Of Authorship

I, Alberto Jesús Uribe Jiménez, declare that this thesis titled, *High Frequency Properties of the Geonium Chip Penning Trap and Development of a Broadband Ion Detection System*, and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualication at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
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UNIVERSITY OF SUSSEX

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SUMMARY:

This thesis presents the development of a novel type of planar Penning Trap known as the Geonium Chip. The thesis describes a wide array of experimental work done in the laboratory in different topics in order to build the trap. The main focus is a detailed research of the high frequency properties of the trap and the design of new methods of detection of the trapped particles.

The Geonium Chip aims at developing a practical planar, scalable Penning Trap making it suitable for new uses and technologies, such as mass spectrometry and single microwave photon detection.

This thesis is mainly focussed on the high frequency properties of the trap, essential to the design of experiment and specially of the chip itself. A new trapped particle detection system is investigated, which replaces the narrow band superconducting resonator normally used in Penning trap experiments by a common SMD resistor. This represents a considerable reduction of the size of the set-up. Moreover, it is an important progress with respect to previous resonator systems, since it is able to work in a broad range of frequencies - a severe limitation of current Penning traps in applications such as mass spectrometry.

Acknowledgements

Firstly, I would like to thank Dr. Jose Verdú Galiana for his time and support. I learnt a lot from him during these years and I really enjoyed working with him. I would also like to thank the rest of the team: Jonathan who showed me all the secrets of the experiment and always remembered any relevant data one could require, April from whom I learnt a lot, Frances that decorated the office with her origami, John who instilled the pie & mash devotion in me, Ryan for making me laugh a lot with his clever but simple jokes that left no stone unturned, and Raquel, who brought new blood into the group. Last but not least, I thank Tomas, who was almost a member of the team. And a grateful acknowledge to all university workers for making everyday work easier.

I dedicate a few words in my mother tongue to the ones that I love: En primer lugar, el mayor de los agradecimientos es para mi familia, muy especialmente a mi padre y madre, abuela y abuelo, a mi hermana, tías, tíos y a mi primo escau. Sin ellos y sin su apoyo incondicional no habría sido posible llegar hasta aquí. También me gustaría agradecer a Miriam por su apoyo, especialmente importante durante los primeros y más duros momentos.

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Chapter 1

Introduction

1.1 Introduction and background

The first Penning trap was built by Hans George Dehmelt, named after the physicist Frans Michel Penning, who proposed a method to increase the lifetime of an electron confined in a vacuum gauge by adding magnetic fields that force the electron to circulate around the lines of field [74].

The first trapping in a Penning trap was completed by Dehmelt and his group in 1973 [98] and, he shared the Nobel prize with Wolfgang Paul in 1989 'for the development of the ion trap technique' [70, 19].

Since then, this technology has progressed enormously. Different models of Penning traps have been developed [32, 7, 46] and the range of applications using it expanded greatly [94]. Current uses of Penning Traps are related to mass spectrometry [20, 86, 3, 100], experiment with antimatter [5, 84], measurements of fundamental constants [44, 86] and g-factor determination [43, 69]. Moreover, there are several proposals to use it in the implementation of quantum computation and other quantum technologies [12].

This thesis is dedicated to study a new type of Penning trap: the *Geonium Chip*. It is a novel prototype of planar and scalable Penning trap, fabricated on a chip where the trap and the magnetic field source are integrated. The Geonium Chip takes its name from the word 'Geonium', which is coined for the first time in 1977 using the prefix 'geo-' as a reference to the earth, according to the authors, "because ultimately the electron is bounded to the earth via the trap structure and the magnet" [21].

1.2 Motivation and applications

Although Penning traps have a broad range of applications, the Geonium Chip is developed mainly focusing in two of them: mass spectrometry and single microwave photon detection. The research done and presented in this thesis is aimed at improving the first one and making possible the second one, with a new implementation using the Geonium chip.

Single microwave photon detection

A well established single microwave photon detection technique is essential for the development of different technologies, specially in the quantum field. Applications have been described related to quantum information, communication and sensing, spectroscopy or search of dark matter particles [71, 34, 60, 17].

Although single photon detection in the optical range is possible and commonly used [41, 23], the detection for itinerant fields in the microwave region is still under development and an approach to this has been exposed only in recent publications [33, 2, 54].

As described in section 2.7, the microwave photon is guided into the cavity, absorbed by the cyclotron frequency of the trapped electron and detected through the axial frequency, providing a non-demolition single microwave photon detection. Therefore, the Geonium chip presents an alternative to develop a compact single microwave photon detector.

Mass spectrometry

Mass spectrometry is an indispensable analytical technique with applications in chemistry, biochemistry, pharmacy or defence, among others [48, 25, 53, 78]. It is a market of USD 4.6 billion with projection of reaching 6.3 USD billion by 2024 [64].

Recent progress in miniaturized mass spectrometers make of them a useful tool in fields such as defence or space [39, 29], however this development has limitations [85, 103]. The Geonium Chip could get a portable device with a good resolution, which overcomes these problems. In addition, it entails a reduction of price, as shown in figure 1.1, with a good resolution, owning a strong position in relation to other technologies.

Fig. 1.1 Estimation of the price and resolution of the Geonium Chip mass spectrometers in relation to other technologies [22].

1.3 Thesis content

This thesis is mainly focused in two goals: analysing the high frequency properties of the chip, which is essential in order to design a trap where the trapped particles can be detected, and a new method of detection of trapped particle, which replaces the big resonator by a small SMD resistor integrated in the chip trap, presenting a clear advantage for many uses, such as mass spectrometry . Additionally, it includes a detail description of the experimental work that has been done in order to build the trap and the beginning of a more advanced research about the set-up used for the coupling of the trapped electrons with microwave photons, which would be necessary for the use of the Geonium Chip as a single microwave photon detector.

The thesis is structured as follows:

- **Chapter 2: Penning Traps and Geonium Chip.** Presents an introduction of the most relevant aspects of the theory of Penning Traps and the Geonium Chip in particular, which represents the basis of what is experimentally developed in the rest of the chapters.

- **Chapter 3: Experimental Set-up.** This chapter includes a detailed explanation to the parts of the experiment that have been developed during this PhD. In addition, there is a brief introduction to the rest of parts that have been developed by other people but it is necessary in order to understand the complete experiment.

- **Chapter 4: High frequency properties of the Geonium Chip.** Chapter 4 is one of the main chapters of the thesis. A very exhaustive analysis of the high frequency

properties of the different chips, that have been designed throughout the years of development of the Geonium Chip experiment, is shown. Some of the most important conclusions of this thesis are given in this chapter.

- **Chapter 5: Detection System.** This is the second main chapter of the thesis. It provides a brief explanation of the current design of the electron detection system and presents the research done in order to get future improvements. By the end of this chapter, a new method of detection is introduced. Although it is not installed in the experiment as it is still being developed, the measurements show a promising result that could minimize the size and present some clear advantages to the current methods of detection in Penning Traps.

- **Chapter 6: Coupling electrons with microwave photons.** The first steps of the development of the set-up that will guide microwave photons into the cavity of the Geonium Chip are introduced in this chapter, which is necessary in order to make the microwave photon detection possible.

Chapter 2

Penning traps and Geonium Chip

This chapter provides a general description of the basic theory of the Geonium Chip. It firstly outlines the principles of the common Penning traps and secondly focuses on the particularities of the Geonium chip as a planar Pening trap. The next chapter provides more details about the experimental set-up of the Geonium Chip, while this chapter has been written from a theoretical perspective.

2.1 Penning trap

The Penning trap is a device used to trap charged particles, such as ions or a single electron in the case of the experiment presented in this thesis, with static magnetic and electric fields. The electrostatic field is created by a group of electrodes connected to different potentials. A cylindrical Penning trap is shown in Figure 2.1, where a typical Penning trap with five electrodes can be observed: one central known as "Ring electrode", two "End-cap electrodes" at both ends of the trap and two "Correction electrodes" between the Ring and the End-cap electrodes. The axis of the cylinder and the magnetic field are orientated parallel to the Z axis and therefore the device is axially symmetrical around it [88].

The charged particle is confined by a quadrupolar electric field in a potential well along Z axis and in any other direction perpendicular to this Z axis by an homogeneous magnetic field. It needs to use both fields in superposition to trap particles in order to agree with Earnshaw's theorem, which is discussed below.

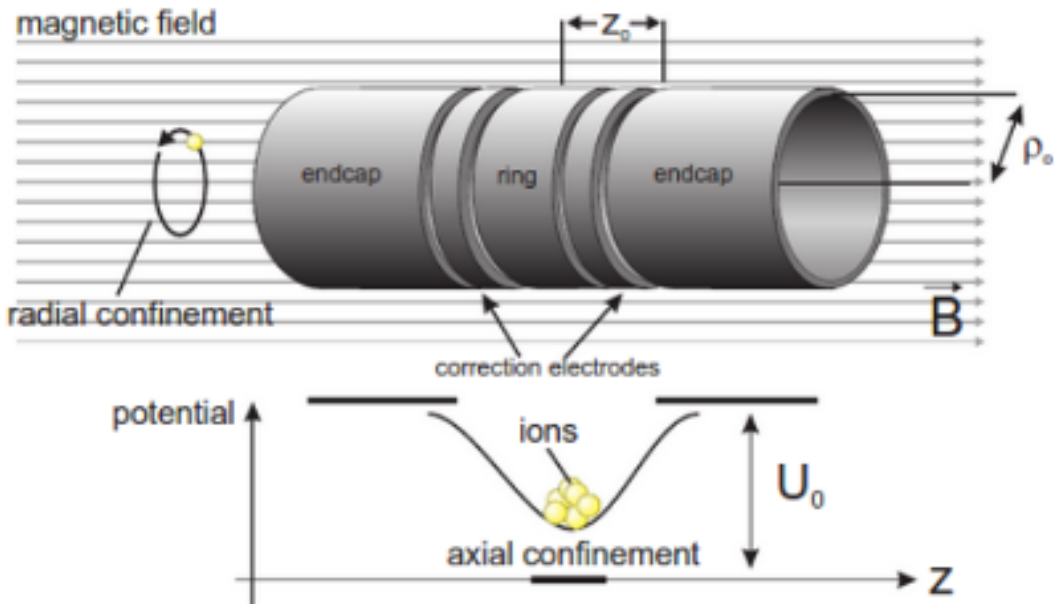


Fig. 2.1 Typical geometry of the cylindrical Penning trap [95].

Earnshaw's theorem

Earnshaw's theorem states that a charged body can not be in an equilibrium position created only by electrostatic fields [16].

Firstly, in order to have an equilibrium position the electric field force would need to point towards this position in every direction, which means that the sign of the divergence of the force must be negative at the equilibrium point.

Secondly, from Gauss's law it is known that the divergence of the force $\boldsymbol{F}$ created by any electric field is zero at any point in free space. Considering Φ the potential associated with the electric field that creates the force F and following the Laplace equation

$$\boldsymbol{\nabla F} = -\nabla^2\Phi = 0, \tag{2.1}$$

there is no possible value for the potential that agrees with the first condition.

In conclusion, both premises can not be fulfilled simultaneously. Therefore there is no possible equilibrium position created only by electrostatic fields [16]. Thus, the conditions to confine a charged particle could be generated by a dynamic electric field, which is the case of Paul traps, or a combination of static electric and magnetic fields, as used in Penning Traps.

2.1.1 The ideal axially symmetrical Penning trap

The potential generated by the electrodes in the Penning trap is [55, 56]

$$\Phi(x_1 y, z) = \frac{U}{2z_0^2 + r_0^2}(2z^2 - x^2 - y^2), \tag{2.2}$$

U being the potential created between the electrodes of the trap, r_0 the distance between the centre of the trap and the Ring electrode and z_0 the distance from the End-cap electrodes to the centre of the trap (figure 2.2). This is the equation of a potential well in the Z direction, which creates an electric field such as $\boldsymbol{E} = -\boldsymbol{\nabla}\Phi$, confining the particle within a line parallel to the Z axis, but not in any other direction.

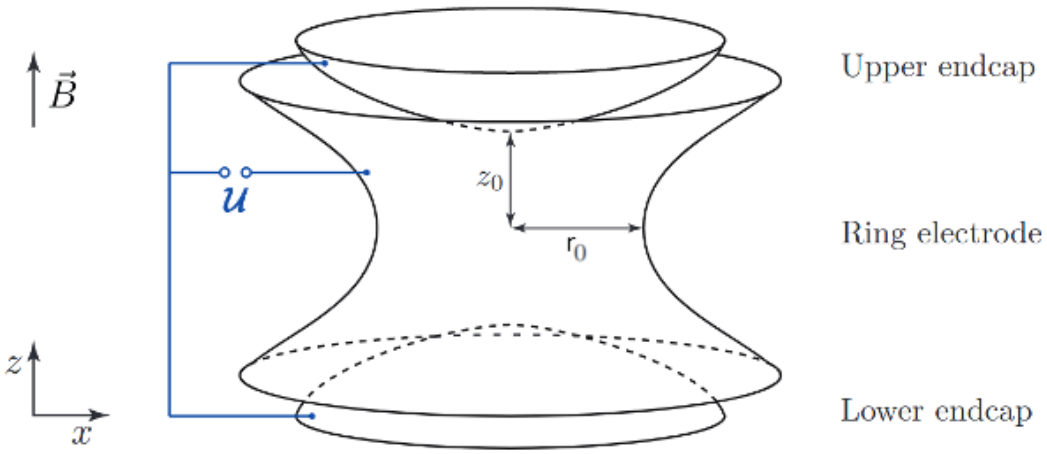


Fig. 2.2 Hyperbolic Penning trap electrodes and magnetic fields [90].

In order to confine the particle in any direction perpendicular to Z, a magnetic field is introduced. This magnetic field is orientated parallel to the Z axis as $\boldsymbol{B} = B_z \hat{u}_z$ [55], confining the particle as required by forcing it to follow a circular trajectory around a line parallel to the magnetic field.

Then, the Lorentz force created over the charged particle by the combination of electric and magnetic fields is

$$\boldsymbol{F} = -q\boldsymbol{\nabla}\Phi + q\left(\dot{\boldsymbol{x}} \times \boldsymbol{B}\right). \tag{2.3}$$

In order to estimate the different frequencies of the particle oscillation within the trap, two different frequencies are considered: the frequency associated with an electrostatic force similar to the one described above, known as the axial frequency (ω_z) and the one

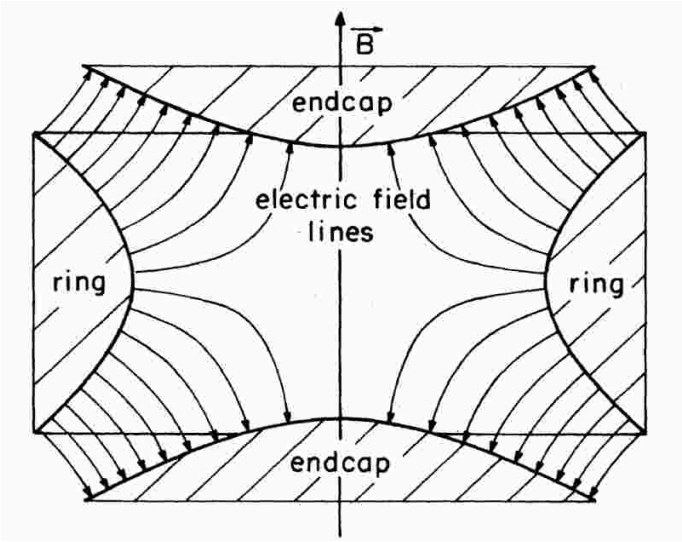


Fig. 2.3 Electrodes, electric and magnetic fields in a hyperbolic Penning trap [7].

associated with the magnetic force, which is the free cyclotron frequency (ω_c). Both of them are equal to

$$\omega_z = \sqrt{\frac{4qU}{m\left(2z_0^2 + r_0^2\right)}} \tag{2.4}$$

and

$$\omega_c = qB/m, \tag{2.5}$$

obtaining the following equation of motion

$$\ddot{x} - \omega_c \dot{y} - \frac{1}{2}\omega_z^2 x = 0, \tag{2.6}$$

$$\ddot{y} - \omega_c \dot{x} - \frac{1}{2}\omega_z^2 y = 0, \tag{2.7}$$

$$\ddot{z} + \omega_z^2 z = 0, \tag{2.8}$$

that can be expressed as

$$\ddot{u} + i\omega_c \dot{u} - \frac{1}{2}\omega_z^2 u = 0, \tag{2.9}$$

where $u = x + iy$ [55]. The general solution for this equation is

$$u(t) = A_+ e^{-i\omega_+ t} + A_- e^{-i\omega_- t}, \tag{2.10}$$

with the modified cyclotron frequency ω_+ and magnetron frequency ω_- equal to

$$\omega_+ = \frac{1}{2}(\omega_c + \omega_1) \tag{2.11}$$

and

$$\omega_- = \frac{1}{2}(\omega_c - \omega_1) \tag{2.12}$$

where [55, 15]

$$\omega_1 = \sqrt{\omega_c^2 - 2\omega_z^2}. \tag{2.13}$$

According to these equations, the trapped charged particle has three distinct motions: a linear one known as axial motion, which is parallel to the Z axis with frequency ω_z; and two circular motions, the modified cyclotron motion, with frequency ω_+ and amplitude A_+, and the magnetron motion, with frequency ω_- and amplitude A_-. A representation of these trajectory described can be observed in figures 2.4 and 2.5.

The trapping condition calculated in [55] from equation 2.9, in agreement with equation 2.13, is

$$\omega_c^2 - 2\omega_z^2 > 0. \tag{2.14}$$

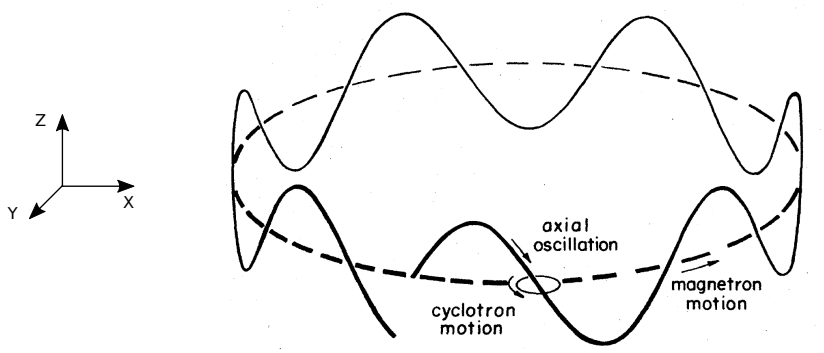


Fig. 2.4 Trajectory of a particle in a Penning trap. Three frequencies are represented: axial, magnetron and cyclotron [7].

2.1.2 The ideal elliptical Penning trap

The potential described in equation 2.2 is created by an ideal axially symmetrical Penning trap. However, this is not the case of the Geonium Chip trap (described in section 2.2) as it is asymmetric along the Y axis, and therefore the theory of elliptical Penning traps must be considered.

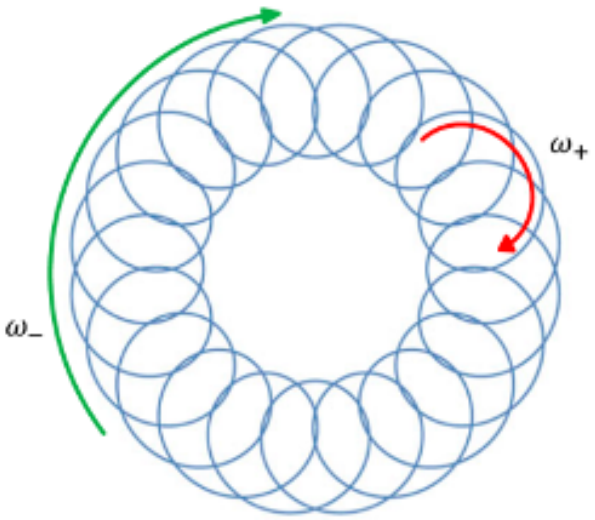


Fig. 2.5 Projection of the trajectory in the XY plane. Two frequencies are visible: magnetron and cyclotron [15].

The potential applied in this case differs from equation 2.2 in a new term that modifies the circular symmetry of the ideal trap. The degree of the deformation of the circular orbit into elliptical by this new term is determined by the ellipticity parameter ϵ. Hence, according to Kretzschmar [56], the potential energy of a charged particle in an elliptical Penning trap including the new ellipticity term is written as

$$V(x,y,z) = \frac{1}{4}m\omega_z^2\left(2z^2 - x^2 - y^2\right) + \frac{1}{4}m\omega_z^2\epsilon\left(x^2 - y^2\right). \tag{2.15}$$

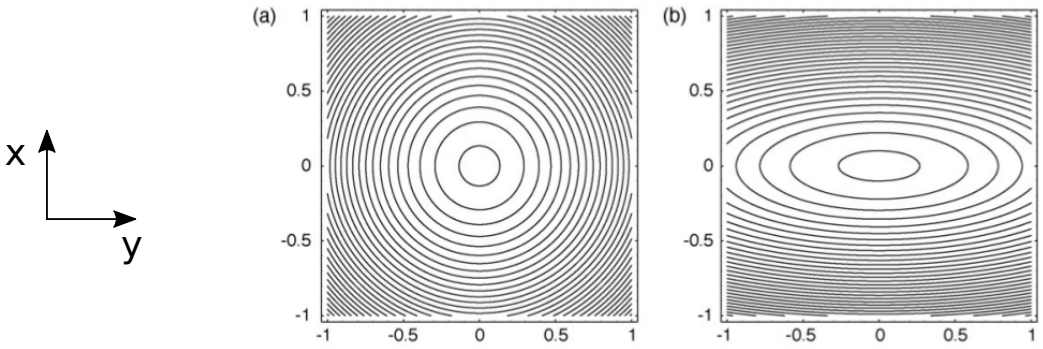


Fig. 2.6 Equipotential lines for a) an ideal Penning trap and b) an elliptical Penning trap [56].

Clearly, if $\epsilon = 0$, the orbit of the trapped particle is not elliptical and the equation 2.15 is equal to the equation of an axially symmetrical Penning trap; if $|\epsilon| > 1$ the trap does not exist. Therefore, the value of ϵ must be $0 < |\epsilon| < 1$. The length of the X axis of the ellipse

would be longer than the length of the Y axis if $\epsilon > 0$, and the opposite would happen when $\epsilon < 0$ [56, 93].

The modified cyclotron frequency $\tilde{\omega}_+$ and magnetron frequency $\tilde{\omega}_-$ of the trapped particle in the elliptical case also depend on the ellipticity parameter and are described as [56]

$$\tilde{\omega}_+ = \sqrt{\frac{1}{2}\left(\omega_c^2 - \omega_z^2\right) + \frac{1}{2}\sqrt{\omega_c^2\omega_1^2 + \epsilon^2\omega_z^4}} \tag{2.16}$$

and

$$\tilde{\omega}_- = \sqrt{\frac{1}{2}\left(\omega_c^2 - \omega_z^2\right) - \frac{1}{2}\sqrt{\omega_c^2\omega_1^2 + \epsilon^2\omega_z^4}} \tag{2.17}$$

where the definitions of ω_c and ω_1 are given by equations 2.5 and 2.13 respectively. The axial frequency is [93]

$$\omega_z = \sqrt{2C_{002}\frac{q}{m}}. \tag{2.18}$$

C_{002} being a coefficient obtained from the series expansion of the potential and related to the curvature of the potential in a direction parallel to the Z axis. It is mathematically described in section 2.2.2.

The ellipticity parameter can be obtained from the values of the frequencies as [76]

$$\epsilon = \pm\frac{\sqrt{\left(\omega_+^2 - \omega_-^2\right)^2 - \omega_c^2\omega_1^2}}{\omega_z^2}, \tag{2.19}$$

obtained from equations 2.16 and 2.17.

At this point two parameters $\eta_\pm$ and $\xi_\pm$ are introduced to simplify the equations [56]

$$\xi_\pm = \sqrt{\frac{\omega_c^2 + \epsilon\omega_z^2 \pm \sqrt{\omega_c^2\omega_1^2 + \epsilon^2\omega_z^4}}{2\omega_+/\omega_1\sqrt{\omega_c^2\omega_1^2 + \epsilon^2\omega_z^4}}}; \quad \eta_\pm = \sqrt{\frac{\omega_c^2 - \epsilon\omega_z^2 \pm \sqrt{\omega_c^2\omega_1^2 + \epsilon^2\omega_z^4}}{2\omega_+/\omega_1\sqrt{\omega_c^2\omega_1^2 + \epsilon^2\omega_z^4}}}. \tag{2.20}$$

The motion equations for the particle in elliptical traps, including the new parameters of equation 2.20, are [56, 93, 76]

$$x(t) = A_+\xi_+ cos(\omega_+ t) + A_-\xi_- cos(\omega_- t), \tag{2.21}$$

$$y(t) = A_+\eta_+ sin(\omega_+ t) + A_-\eta_- sin(\omega_- t), \tag{2.22}$$

$$z(t) = A_z cos(\omega_z t), \tag{2.23}$$

where the amplitudes A_+, A_- and A_z are [56, 93, 76]

$$A_+ = \frac{1}{\omega_+}\sqrt{\frac{2E_+}{\gamma_+ m}}; \quad A_- = \sqrt{\frac{2E_-}{\left(\omega_-^2 - \omega_z^2/2\right)m}}; \quad A_z = \frac{1}{\omega_z}\sqrt{\frac{2E_z}{m}}; \tag{2.24}$$

with $\gamma_+ = 1 - \frac{\omega_z^2}{2\omega_+^2} \approx 1$ and the cyclotron and magnetron energies represented by E_+ and E_- respectively.

2.1.3 The invariance theorem

From equations 2.16 and 2.17 the cyclotron and magnetron frequencies dependence on the ellipticity parameter can be written as [56, 7]

$$\tilde{\omega}_+^2 = \omega_+^2 + \kappa\omega_1 K(\epsilon) \tag{2.25}$$

and

$$\tilde{\omega}_-^2 = \omega_+^2 - \kappa\omega_1 K(\epsilon). \tag{2.26}$$

With some simple algebraic calculations of these equations, the agreement with the invariance theorem firstly introduced in [7] can be verified

$$\tilde{\omega}_+^2 + \tilde{\omega}_-^2 + \omega_z^2 = \omega_+^2 + \omega_-^2 + \omega_z^2 = \omega_c^2. \tag{2.27}$$

Therefore the free cyclotron frequency ω_c can be measured from the values of ω_+, ω_- and ω_z. It has been used in many applications [31], such as the experiments for the most precise measurements of magnetic moment of a free electron [42] or g-factor of ions [47, 87, 80, 27].

2.2 The Geonium Chip trap

The conception of the Geonium Chip is based on the idea of a planar and compact Penning trap with five electrodes. It is conceived as a projection over a flat surface of the electrodes of a cylindrical Penning trap, as shown in figure 2.7.a. It is a coplanar-waveguide (CPW) [79] Penning trap, where the coordinate system is positioned, as it can be seen in figure

2.7.a., with the origin over the centre of the surface of the Ring electrode, the Y axis perpendicular to the plane and the Z axis parallel to the plane and the electrodes.

As described in the case of a standard cylindrical Penning trap, the trapped particle in this planar Penning trap is confined by a combination of electric and magnetic fields. However, in this case these fields have to be analysed carefully as they are created differently due to the particularities of a planar trap.

- The electrostatic field is created by planar electrodes (figures 2.7.b and 2.8). It means that the trapped particle is not surrounded by electrodes, breaking the symmetry between the Y and X axis, which is characteristic of an elliptical Penning trap that follows the equations described in section 2.1.2.
- The magnetic field is generated by a planar magnetic field source attached to the bottom of the chip that creates a magnetic field parallel to the Z axis, as shown in figure 2.7.b. The technical details of this source are described in chapter 3

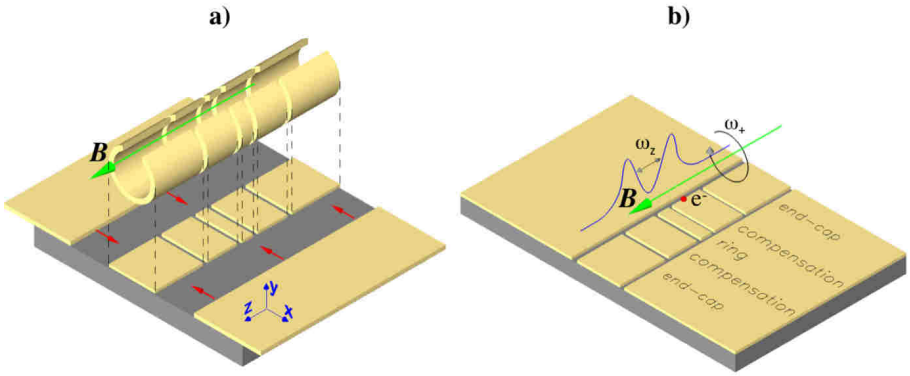


Fig. 2.7 a) Projection of a cylindrical five-pole Pening trap over a planar surface. b) Representation of the potential and magnetic field created by the Geounium Chip system and cyclotron and axial motions of the trapped particle [93].

2.2.1 Electrostatic field

As in any other Penning trap, the potential generated by the Geonium Chip electrodes is a potential well in the Z direction, with the minimum potential over the centre of the trap. However, this is not a minimum in every direction, as proved by the Earnshaw's theorem. Figure 2.9 shows a representation of the minimum described.

The equation of trapping potential created by the chip can be written as

$$\phi(x,y,z) = V_r \cdot f_r(x,y,z) + V_c \cdot f_c(x,y,z) + V_e \cdot f_e(x,y,z) + f_{gaps}(x,y,z|V_r,V_c,V_e), \quad (2.28)$$

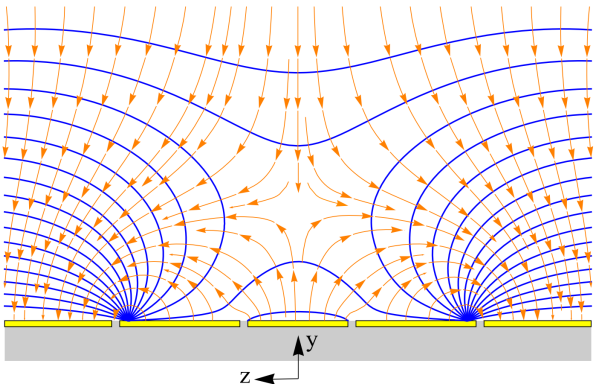


Fig. 2.8 Equipotential lines and electric field created by the Geonium chip Penning Trap [1].

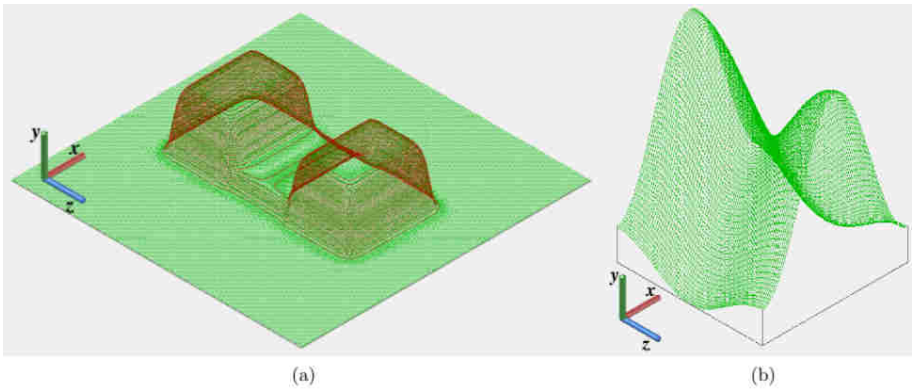


Fig. 2.9 a) Potential generated by the Geonium chip close to the surface of the chip. b) Potential at the trapping height y_o [75].

where f_r, f_c, f_e and f_{gaps} are functions dependent on the dimensions of the trap exclusively, except for f_{gaps}, which also depends on the voltages applied to the electrodes. Their expressions are given in [93]. V_r, V_c and V_e, shown in figure 2.10, represent the DC voltages applied to the Ring, Corrections and End-caps electrodes respectively. From these voltages, the tuning ratio $T_c = V_c/V_r$ and the End-cap to Ring voltage ratio $T_e = V_e/V_r$ are defined [93].

The equilibrium position of the trap in the Y axis is defined as the point y_0 and is calculated as follows

$$\left.\frac{\partial\phi(0,y,0)}{\partial y}\right|_{y=y_0} = \left.\frac{\partial f_r}{\partial y}\right|_{y=y_0} + T_c\left.\frac{\partial f_c}{\partial y}\right|_{y=y_0} + T_e\left.\frac{\partial f_e}{\partial y}\right|_{y=y_0} = 0. \tag{2.29}$$

Hence, this equilibrium position $y_0(T_c, T_e)$ depends on the value of the ratios $T_e = V_e/V_r$ and $T_c = V_c/V_r$. 'T_c' is known as a 'Tuning ratio' and plays a similar role as the ratio introduced in [7].

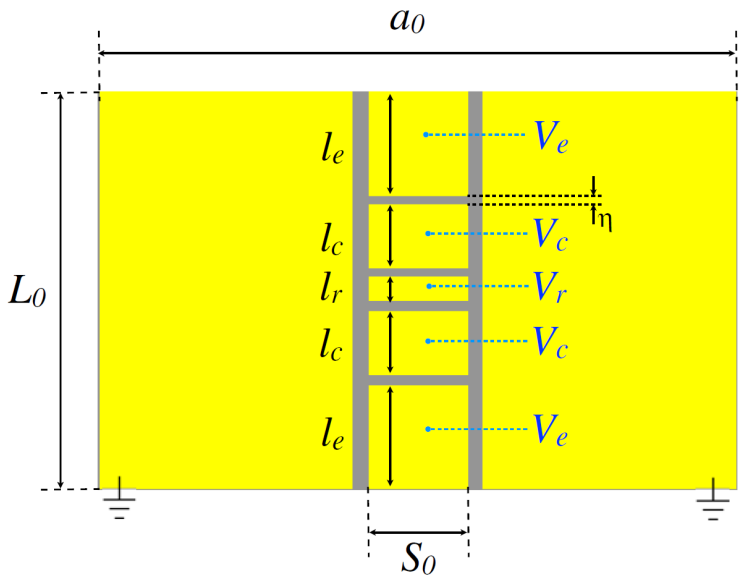


Fig. 2.10 Applied voltages to the geonium chip electrodes[93].

2.2.2 Coefficients theory

The series expansion of $\phi(x,y,z)$ around the equilibrium point (0,y_0,0) (figure 2.11) is given in [93], considering only terms up to the fourth order

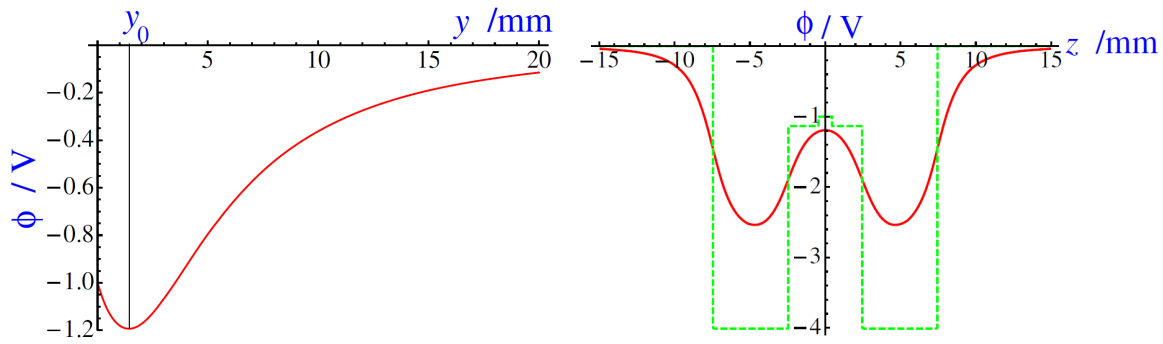
$$\begin{aligned}\phi(x,y,z) = \phi(0,y_0,0) + ... + \underbrace{C_{002}z^2 + C_{200}x^2 + C_{020}(y-y_0)^2}_{\phi_{quad}} \\ + \underbrace{C_{012}z^2(y-y_0) + C_{210}x^2(y-y_0) + C_{030}(y-y_0)^3}_{\text{Odd anharmonicities}} \\ + \underbrace{C_{202}z^2x^2 + C_{002}z^2(y-y_0) + C_{220}x^2(y-y_0)^2 + C_{004}z^2 + C_{400}x^4 + C_{400}x^2(y-y_0)^4}_{\text{Even anharmonicities}},\end{aligned} \tag{2.30}$$

where the expansion coefficients are defined in [93]

$$C_{ijk} = \frac{1}{i!j!k!} \cdot \frac{\partial^{i+j+k}\phi(x,y,z)}{\partial x^i \partial y^j \partial z^k}\bigg|_{(0,y_0,0)}. \tag{2.31}$$

In this equation, the $C_{i,j,k}$ coefficients are equal to zero for odd values of i and k, due to the symmetry of the potential $\phi(x,y,z)$ along the X and Z axes (figure 2.11)[93].

Applying the Laplace equation $\nabla^2\phi(x,y,z) = 0$ to the series expansion of the potential of equation 2.30, the following expressions of the coefficients can be obtained



a) b)

Fig. 2.11 a)Potential along the Y axis over the centre of the chip. b)Potential along the Z axis [93].

$$\begin{aligned} C_{200} + C_{020} + C_{002} &= 0, \\ 3C_{030} + C_{210} + C_{012} &= 0, \\ 6C_{400} + C_{220} + C_{202} &= 0, \\ 6C_{040} + C_{220} + C_{022} &= 0, \\ 6C_{004} + C_{202} + C_{022} &= 0, \end{aligned} \tag{2.32}$$

and the value of ϕ_{quad} is

$$\phi_{quad} = C_{002}\left(z^2 - \frac{x^2 + (y - y_0)^2}{2}\right) + \frac{1}{2}C_{002}\epsilon \cdot \left(x^2 - (y - y_0)_2\right), \tag{2.33}$$

where $\epsilon = \frac{C_{200} - C_{020}}{C_{002}}$ is the ellipticity parameter [93]. The ellipticity parameter has the value $\epsilon = 0$ if $C_{200} = C_{020}$, which is the case of axially symmetrical Penning traps, described in section 2.1.1. However the Geonium chip follows the case of the elliptical Penning trap, since in general $\epsilon \neq 0$ [56, 93].

2.2.3 Anharmonicities

The anharmonicities of the trap will shift the frequencies of the particle depending on the energies

$$\begin{pmatrix} \Delta\nu_p \\ \Delta\nu_z \\ \Delta\nu_m \end{pmatrix} = \underbrace{\begin{pmatrix} M_{1,1} & M_{1,2} & M_{1,3} \\ M_{2,1} & M_{2,2} & M_{2,3} \\ M_{3,1} & M_{3,2} & M_{3,3} \end{pmatrix}}_{\text{M frequency-shift matrix}} \begin{pmatrix} \Delta E_p \\ \Delta E_z \\ \Delta E_m \end{pmatrix}, \tag{2.34}$$

the effect of the anharmonicities being represented by the M matrix, which is given by the sum

$$M = M^{012} + M^{210} + M^{030} + M^{220} + M^{202} + M^{022} + M^{004} + M^{400} + M^{040}, \tag{2.35}$$

where each matrix M^{ijk} is associated to a perturbation C^{ijk} of ϕ_{quad}, according to equation 2.30 [93]. The expressions of the coefficients of the matrices M^{ijk} are described in [93].

Since the only frequency directly detected in the case of the electrons is the axial frequency ω_z, keeping this as stable as possible is essential. An important element to consider is the axial energy, which can be affected by thermal fluctuation if the anharmonicities are not cancelled, causing variations on the axial frequency.

The dependence of the axial frequency on the axial energy is related to the matrix element $M_{2,2}$. Therefore, this section includes an analysis of this matrix, which, according to the expressions of the matrices M^{ijk} given in [93], can be calculated by only considering the matrices ${M_{2,2}}^{004}$ and ${M_{2,2}}^{012}$ as

$${M_{2,2}}^{004} = -\frac{3q}{16\pi^4 m^2 \nu_z^3} C_{004} \tag{2.36}$$

and

$${M_{2,2}}^{012} \simeq \frac{q^2 \eta_m^2}{32\pi^6 m^3 \nu_z^5} C_{012}^2. \tag{2.37}$$

The optimal tuning ratio

Following what has been described above, by making the value of the matrix $M_{2,2} = 0$, the dependence of the axial frequency on the axial energy $\frac{\Delta\nu_z}{\Delta E_z}$ can often be eliminated. This happens for a particular value of the tuning ratio, that is known as the "optimal tuning ratio" T_c^{opt} [93].

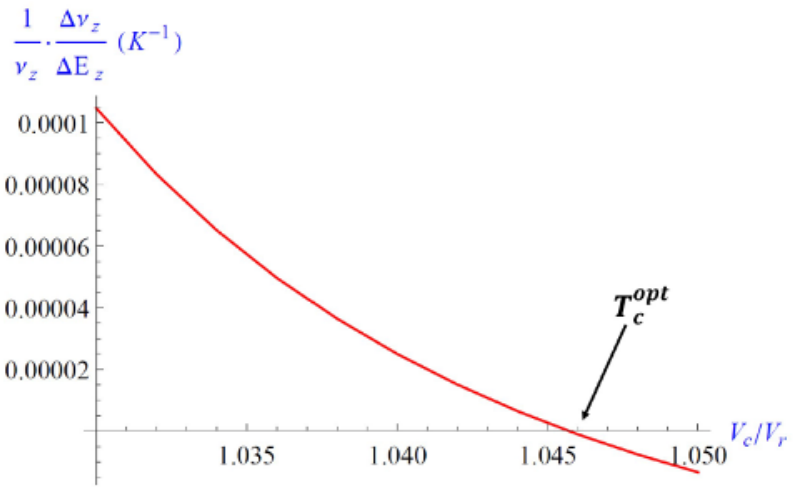


Fig. 2.12 Calculation of $M_{2,2}$ as a function of T_c. The value of T_c^{opt} is indicated at the point where $M_{2,2} = 0$ [14].

The T_c^{opt} eliminates $M_{2,2}$ only in a particular range, known as "useful trapping interval". In figure 2.13 from the example of [76], the value of T_c^{opt} is represented as a function of y_0, for the ratio $T_g = V_g/V_r = 0$, where V_g is the voltage applied to the Ground Plane. Since y_0 can be modified by changing the values of T_c and T_e, the voltages V_c and V_e must be chosen such that the height of the trapped particle y_0 is within this range. Otherwise an accurate measurement of the axial frequency would not be possible [93, 76, 14].

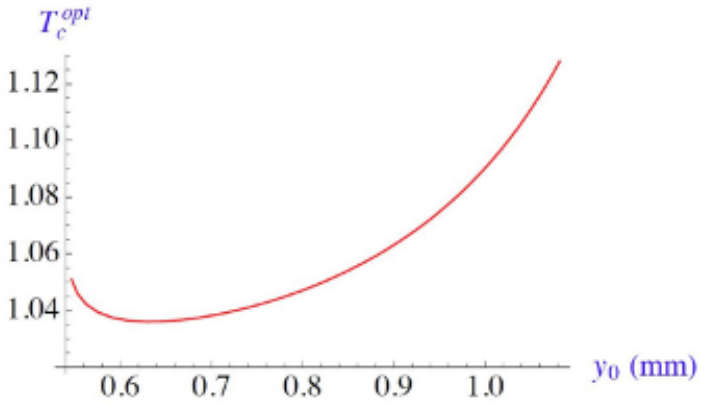


Fig. 2.13 Useful trapping interval for the example CPW-trap described in [76]. Calculation of T_c^{opt} as a function of y_0 for $T_g = V_g/V_r = 0$.

2.2.4 The side electrodes

The side electrodes are two electrodes placed on the sides of the trap as shown in figure 2.14. These two electrodes were included in the first versions of the Geonium Chip,

but they have been removed from the latest designs for simplicity, since it is not an essential part to trap. However this discussion is of interest in this thesis as it could be an improvement for future models of the trap.

The DC voltage applied on these is V_g and the side electrode to Ring voltage ratio is $T_g = V_g / V_r$ [76]. By including the side electrodes, the ellipticity parameter of the trap can be tuned (figure 2.15) and the useful trapping interval can be extended [76].

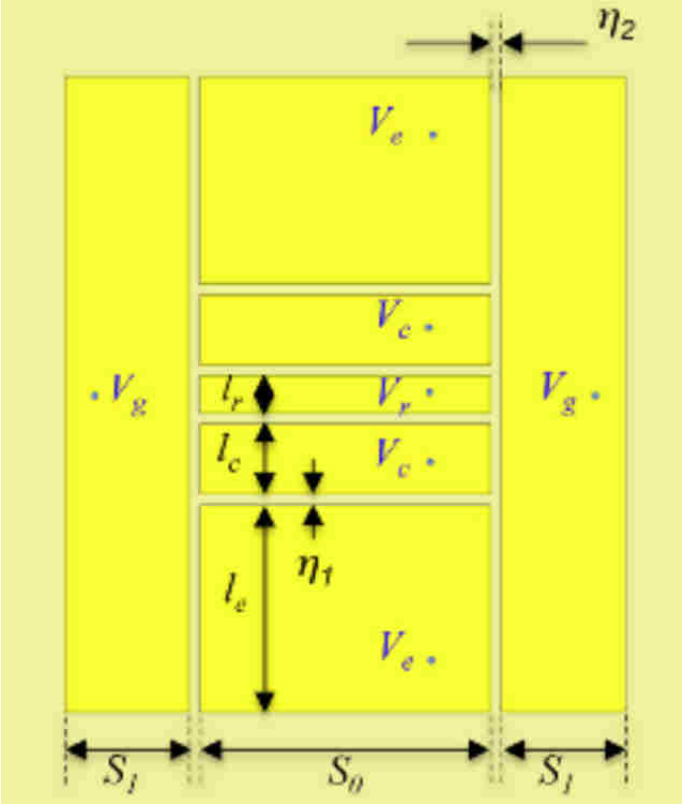


Fig. 2.14 Geonium chip with side electrodes [76].

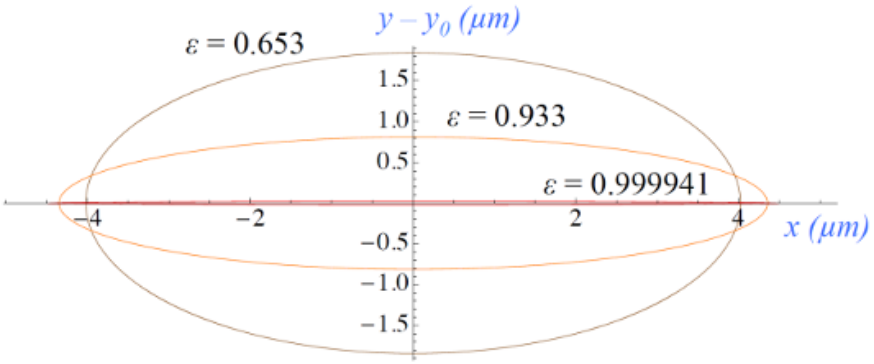


Fig. 2.15 Magnetron orbit of the electron for different values of the ellipticity parameter, tuned by changing the side electrode-to-Ring voltage ratio T_g [76].

The tuning of T_g could make the ellipticity parameter reach values very close to 1, which is known as a ultra elliptical regime [76]. This operation regime could be useful for the Geonium Chip since it completely suppresses the y amplitude of the magnetron motion, considerably reducing the effect of the inhomogeneities of the magnetic field along the Y axis. It has been explained in more detail in [58].

2.3 Loading procedure

The procedure for loading the electrons in the trap is being developed by R. Willetts and J. Pinder, therefore is beyond the scope of this thesis. However, a basic notions will be provided in this section since it is necessary for the complete understanding of the research presented in this thesis.

Firstly, electrons appear in the cavity after being ejected from a target by a UV light beam using photoelectric effect. Thus, the temperature of the ejected electron is

$$T_{electron} = \frac{hf - \Phi}{k_B}, \tag{2.38}$$

where k_B is Boltzmann's constant, hf represents the energy of the UV light photons and Φ the work function of the target material. An experimental analysis of this photoelectric effect is included in section 3.2.

The ejected electrons are confined around the Z axis by a strong homogeneous magnetic field, following a circular trajectory as described in previous sections, and moving through this axis with the kinetic energy provided by the UV light. Some of them will reach the trapping region and will be confined with the procedure described in section 3.3.

2.4 The detection system of the trapped electrons

The non-destructive detection technique used in the Geonium chip experiment is described in this section from a theoretical point of view. Technical details of the actual experimental set-up are discussed in chapter 5.

Destructive techniques destroy the samples of trapped particles by using all or some of them for the detection. Although it is a sensitive and reliable method, the samples are destroyed, so the trap needs to be re-loaded after every detection. Non-destructive

techniques, in contrast, do not use the trapped particles, but the detection is done by measuring the perturbation that the same trapped particle produces. This last case is the one developed in this experiment, where the detection is based on the measurement of the current created by the charges that the trapped ion induces over the electrodes of the trap [52, 51].

2.4.1 Detection of the trapped electron

In our experiment, the trapped electron is detected by measuring the currents that are induced on one of the Correction electrodes, which is used as a detector.

The electron moves at the axial frequency and the distribution of the charge, induced by this electron on the surface of the electrode, changes as shown in figure 2.16. This change causes a movement of charge, creating an AC current with a frequency equal to the axial frequency of the electron, excluding negligible relativistic delays.

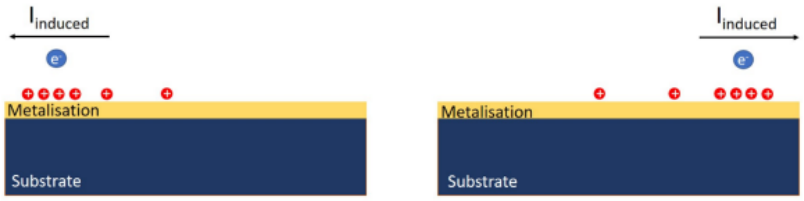


Fig. 2.16 Charges induced by an electron over a metallic surface. The charges change the position as the electron moves [14].

Since the current generated is too small to be detected, a tank circuit is connected to the detection electrode, which is the Correction electrode in this case, and the signal generated across this circuit is amplified several times.

The designed tank circuit is a high Q factor resonator with the resonant frequency equal to the axial frequency of the trapped particle. Hence, if an ion is present in the trap, the Q factor of the resonator would be lower and the particle could be detected. It would be seen as a dip over the resonant curve of the resonator detected by the spectrum analyser, which would indicate that the ions are trapped. The width of the dip would depend on the number of ions in the trap, being the minimum width reached for the limit of one single electron. A detailed explanation of this effect can be seen in section 2.6, where the trapped particle effect is modelled as a capacitor and inductor in parallel to the tank circuit.

The detection set-up, including tank circuit and amplifier, is shown in figure 2.17, whilst the technical details of the actual system designed for the Geonium chip experiment have been described in chapter 5.

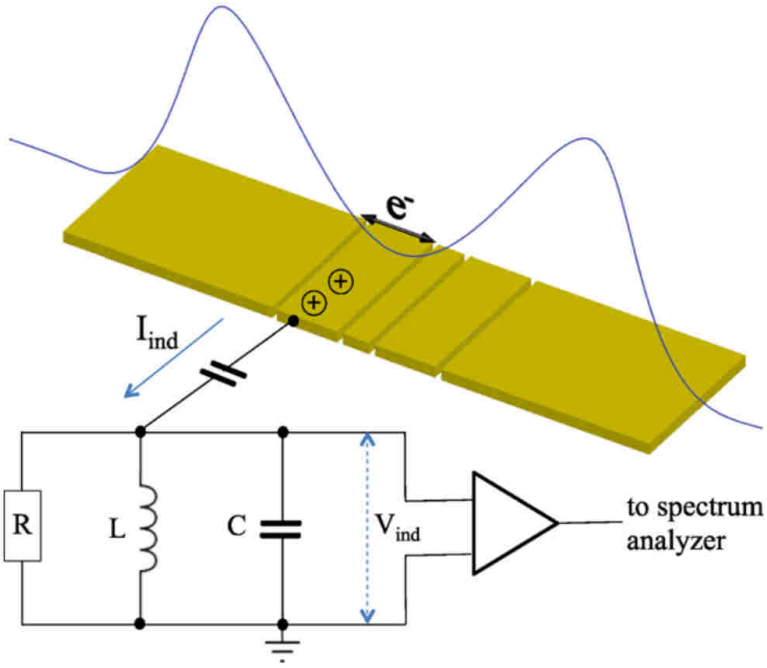


Fig. 2.17 Charge induced on the Correction electrode by the trapped electron. A tank circuit is connected to this electrode for the detection of the axial motion and the signal is sent to the spectrum analyzer amplified by several amplifiers [1].

2.4.2 The induced currents

As described above, the presence of electrons in the trap induces charge on the electrodes. The calculation of this charge is necessary in order to estimate the induced currents.

According to the method of images [11], the perturbation caused by the charge of the trapped ion and the charge accumulated on the conducting surface of the chip could be calculated in a more simplified way, by considering only the charge of the trapped ion placed over the surface of the chip and another charge of equal value to the charge of this ion but with opposite sign and placed at the same distance below the surface of the chip. It is represented in figure 2.18.

This has been calculated in [1] using Green's function for Laplace's equation with Dirichlet's boundary conditions $G(\mathbf{r} \mid \mathbf{r'})$. Assuming that the chip is an infinite plane, this

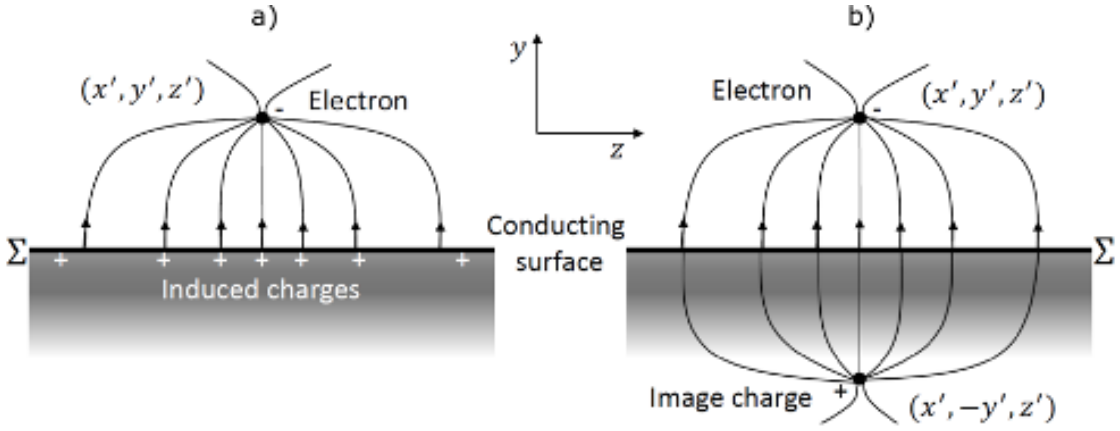


Fig. 2.18 a) Electric field lines and charges induced by the trapped electron. b) Image charge of the electron symmetrically placed to the surface of the chip [58].

function can be written as [1]

$$G(\mathbf{r}|\mathbf{r'}) = \frac{1}{\sqrt{(x-x')^2+(y-y')^2+(z-z')^2}} - \frac{1}{\sqrt{(x-x')^2+(y+y')^2+(z-z')^2}}, \tag{2.39}$$

in order to define the value of the charge

$$q_{ind}(\mathbf{r}(t)) = -q \underbrace{\frac{1}{4\pi}\int\int_{\Sigma} dx'dz' \left.\frac{\partial G(\mathbf{r}(t)|x',y',z')}{\partial y'}\right|_{y'=0}}_{\Lambda_{\Sigma}(\mathbf{r})}, \tag{2.40}$$

where **r'** is the position of the source and **r**(t) is the position of the trapped particle [1]. From this value given by equation 2.40, the induced current is calculated as the variation of charge with time [1]

$$I_{ind}(t) = \frac{dq_{ind}(\mathbf{r}(t))}{dt} = \nabla q_{ind}(\mathbf{r}) \cdot \dot{\mathbf{r}}(t) = \frac{\partial q_{ind}}{dx}\dot{x} + \frac{\partial q_{ind}}{dy}\dot{y} + \frac{\partial q_{ind}}{dz}\dot{z}. \tag{2.41}$$

2.5 Resistive cooling

The dissipation of power in the resonator, produced by the circulation of the induced current through this circuit, could be understood as an external damping force that reduces the energy of the trapped electron. This is a technique known as resistive cooling, since the electron reduces its temperature by loosing it through the resonator circuit.

The motion equation of the trapped particle affected by this resistive cooling force is

$$\ddot{z} = -\omega_z^2 z - \gamma \dot{z} - \frac{qV}{mD_{eff}^z} + \frac{F_{ind}}{m}, \tag{2.42}$$

where $\gamma = \frac{q^2 Z(\omega)}{m\left(D_{eff}^z\right)^2}$ is the damping ratio, representing the cooling ratio of the motion of the particle, and the force induced by the electric field created by ϕ_{ind} is $F_{ind} = -q\boldsymbol{\nabla}\phi_{ind}$ [1].

The potential ϕ_{ind} is generated by the induced currents described in equation 2.41 and its associated voltage V_{ind},

$$\phi_{ind} = -V_{ind} \cdot \Lambda_{\sum}(\mathbf{r}) = qZ(\omega)\Lambda_{\sum}(\mathbf{r})\boldsymbol{\nabla}\Lambda_{\sum}(\mathbf{r}) \cdot \dot{z}, \tag{2.43}$$

where Green's second identity as described in [50] is used in the definition of the factor $\Lambda_{\sum}(\mathbf{r})$, described in equation 2.40 [1]. From equation 2.43, the induced force can be described as [1]

$$\mathbf{F}_{ind} = -q \cdot \boldsymbol{\nabla}\phi_{ind} = -q^2 Z(\omega)\left[\boldsymbol{\nabla}\Lambda_{\sum}(\boldsymbol{\nabla}\Lambda_{\sum} \cdot \dot{\mathbf{r}}) + \Lambda_{\sum}(\dot{\mathbf{r}} \cdot \boldsymbol{\nabla})\boldsymbol{\nabla}\Lambda_{\sum}\right]. \tag{2.44}$$

which is proportional to the velocity of the particle and to the impedance of the resonator circuit. This can also be expressed as

$$\mathbf{F}_{ind} = -q^2 Z(\omega)\mathbf{D}_{eff}^{-1} \cdot \left(\mathbf{D}_{eff}^{-1} \cdot \dot{\mathbf{r}}\right), \tag{2.45}$$

in terms of the three components vector $\mathbf{D}_{eff}^{-1} = \left(\frac{1}{D_{eff}^x}, \frac{1}{D_{eff}^y}, \frac{1}{D_{eff}^z}\right)$ and dismissing part of equation 2.44 in agreement with the "effective coupling distance" approximation, which considers the position of the particle very close to the equilibrium position $\mathbf{r}(t) \approx (0, y_0, 0)$. The equation of the effective coupling distance vector is [1]

$$\mathbf{D}_{eff}^{-1}\left(y_0; \sum\right) = \lim_{\mathbf{r}(t)\to(0,y_0,0)} \boldsymbol{\nabla}\Lambda_{\sum}(\mathbf{r}(t)). \tag{2.46}$$

In the Geonium chip experiment the resistance $Z(\omega)$ is built as a niobium cylindrical helical resonator, designed by J.Pinder [75]. Although it is working correctly, it is one of the biggest devices in the experiment and, in order to reduce this size, other models of

resonator are being tested. The technical details about the resonators are described in chapter 5.1.

Finally, the cooling time constant of this dissipative motion is described in [1, 49] as

$$\tau^i(\omega) = \frac{m}{q^2 Z(\omega)} \left(D^i_{eff}\right)^2. \tag{2.47}$$

2.6 Equivalent circuit

In this section, the effect of the trapped ion detected is modelled as an equivalent electronic circuit.

The movement of a single trapped particle without the resistive cooling force is

$$\ddot{z} = -\omega_z^2 z - \frac{qV}{mD^z_{eff}} + \frac{F_{ind}}{m}. \tag{2.48}$$

The induced force F_{ind} is negligible for a single trapped particle. Therefore, the voltage V for the case of a single ion is [28, 1, 99]

$$V = L_{ion}\frac{di_{ion}}{dt} + \frac{1}{c_{ion}}\int i_{ion}dt, \tag{2.49}$$

where i_{ion} is the current induced by the single trapped particle and $L_{ion} = \frac{m}{q^2}\left(D^z_{eff}\right)^2$, the equivalent inductance, with a resonant frequency $\frac{1}{\sqrt{L_{ion}\cdot C_{ion}}} = \omega_{ion}$. The equivalent inductance L_{ion} and capacitance C_{ion} of the trapped particle appear in parallel to the resonator, as shown in figure 2.19.

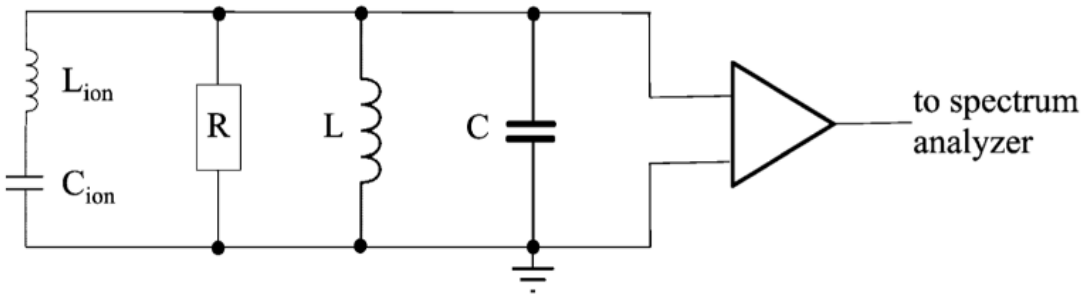


Fig. 2.19 Equivalent circuit to the trapped ion [1].

In the case of n trapped particle, the induced current is $I_n = n \cdot i_s$. Hence, the value of its equivalent circuit components are $L_n = L_{ion}/n$ and $C_n = C_{ion}/n$. The impedance of this

equivalent circuit is

$$Z_\omega = \frac{1}{\frac{1}{j\omega L_n + \left(\frac{1}{j\omega C_n}\right)} + \frac{1}{R} + \frac{1}{j\omega L} + j\omega C}. \tag{2.50}$$

A representation of this impedance as a function of frequency can be observed in figure 2.20, where the dependence of the dip width $\Delta\nu$ on the number of trapped particles n can be observed. Using the cooling time constant, this width can be expressed as [1, 99]

$$\Delta\nu = \frac{1}{2\pi\tau}. \tag{2.51}$$

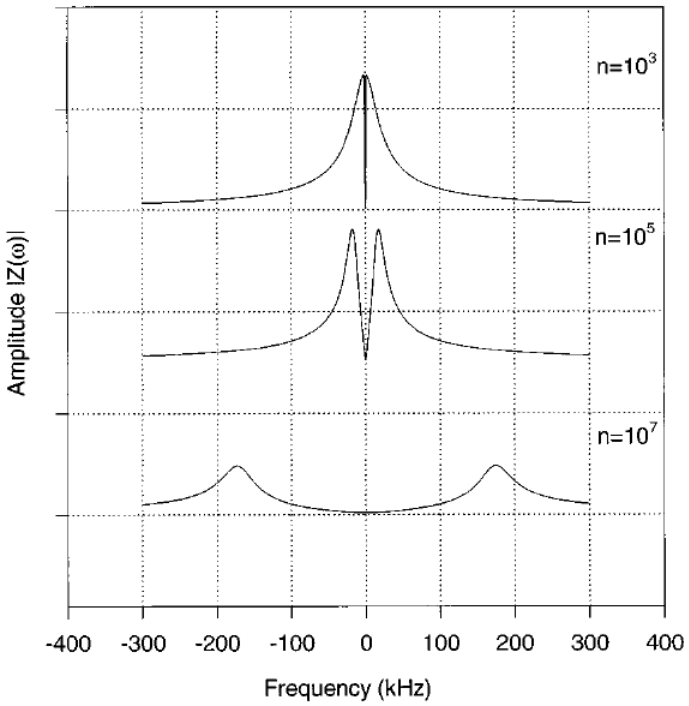


Fig. 2.20 Simulation of the impedance of equation 2.50 [28].

2.7 Detection of microwave photons with the trapped electron

One of the most important and innovative applications of the Geonium Chip trap is the detection of single microwave photons. In this section a theoretical approach to the problem is provided, while a more practical development of the system is presented in chapter 6 from a experimental point of view. In order to use the trapped electron as a microwave photon detector, a set-up is required that facilitates the interaction of these

photons with the cyclotron motion of the electron [1]. The details of both, the detection and the required set-up, are given below.

2.7.1 Set-up of the microwave photon detector

Firstly, a cryogenic vacuum chamber made of a conductor material is attached to the top of the Geonium chip, enclosing the trapping region and creating a microwave cavity with the conductive surface of the chip, as shown in figure 2.21. A detailed description of the actual cryogenic chamber installed in the experiment can be found in the section 3.1. This chamber would be designed such that the frequencies of the microwave radiation that the system is detecting do not match with the resonant frequencies of the cavity. Therefore, due to the Purcell effect, the spontaneous emission of cyclotron radiation is inhibited, as proved in [73, 1].

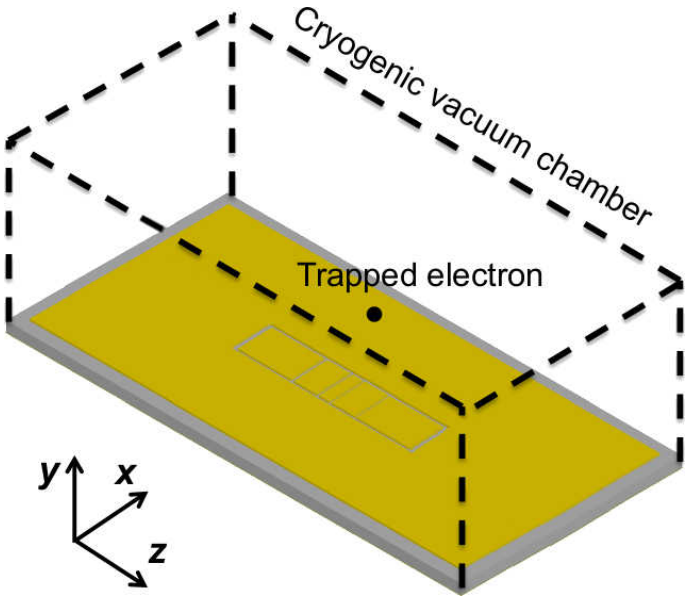


Fig. 2.21 Trapped electron in the cavity created between the conductive top of the chip and the conductive chamber.

Secondly, a waveguide should be installed in order to transmit the photons that need be detected. Thus, the spontaneous emission of energy from the cyclotron oscillation is not inhibited at the frequencies propagated through the waveguide, making possible the detection of these photons. Different kinds of waveguide could be used for this purpose, for instance a Coplanar-waveguide is presented in [1]. The solution proposed and described in chapter 6 consists of an antenna that is installed in the cavity and creates a field which interacts with the electron. The field emitted by this antenna is linearly

polarized, hence no fields with different polarization would perturb the electron. The details of the interaction between this photon and the trap electron are described in section 2.7.2.

2.7.2 Photon-electron interaction

Since the cyclotron motion of the electron ω_c is in the frequency range of microwaves, it could interact with the microwave photons and, therefore, it could be used for detection, which is detailed in section 2.7.3. The cyclotron frequency of the electron can be approximated to the free cyclotron frequency for fields above 0.1 T [13]

$$\omega_p \simeq \omega_c = \frac{q}{m} B_0. \tag{2.52}$$

As explained in [13, 7], the electron's spin intrinsic dipole moment could also provide a possible transition, however, it is a magnetic dipole transition, which is extremely weak comparing to the electric dipole transition of the interaction with the cyclotron motion.

The Hamiltonian of the interaction between two harmonic oscillators, that is, the cyclotron motion of the trapped electron and the radiation field, is [13, 26]

$$H = \hbar\omega_p \left(a_p^\dagger a_p + \frac{1}{2} \right) + \hbar\omega_{MW} \left(a_{MW}^\dagger a_{MW} + \frac{1}{2} \right) + \hbar\Omega \left(a_{MW}^\dagger a_p + a_{MW} a_p^\dagger \right), \tag{2.53}$$

where $\hbar$ is the reduced Planck's constant, $a_p^\dagger$ and a_p are the creation and annihilation operators of the cyclotron degree of freedom, $a_{MW}^\dagger$ and a_{MW} are the creation and annihilation operators of the propagating microwave mode and Ω is the coupling strength [13].

The power of the microwave in the CPW transmission line of the trap is [13]

$$P_{MW} = \frac{1}{2} |V_\gamma|^2 Y_{in} = \frac{\hbar\omega_{MW}}{\tau_{MW}}, \tag{2.54}$$

where V_γ is the difference of potential between the strip that transport the microwave and the Ground Plane electrodes, produced by the microwave photons, which enter into the trap with a rate equal to $1/\tau_{MW}$. $\hbar\omega_{MW}$ is the energy of every photon and Y_{in} is the input admittance of the CPW transmission line with the trapped electron.

The probability that the electron absorbs a microwave photon transmitted by the CPW line, producing a transition in the cyclotron quantum state of the electron from $|0\rangle$ to $|1\rangle$,

is calculated in [13] using Fermi's golden rule as

$$\Gamma_{|0\rangle\to|1\rangle} = \frac{2\pi}{\hbar}\left|\langle 0|\,\vec{E}\cdot\vec{P}\,|1\rangle\right|^2 g_p(E) = \frac{2\pi}{q}^2 {V_\gamma}^2\hbar|\langle 0|\,E^{even}_{CPW}\cdot\vec{p}\,|1\rangle|^2 g_p(E), \tag{2.55}$$

where $g_p = \frac{1}{2\pi\hbar\omega_p}$ is the density of final available energy states for the cyclotron motion, $\vec{P} = q(X,Y,Z)$ its the electric dipole momentum operator, and $\vec{E} = V_\gamma\left(E^{even}_{CPW}, E^{odd}_{CPW}, 0\right)$ is the electric field composed of two components, as the CPW transmission line has two propagation modes. More details of this electric field have been included in Appendix A.

2.7.3 Microwave photon detection

The absorption of microwave photons is detected by using *The Continuous Stern-Gerlach Effect* [18]. For this purpose, a *magnetic bottle* configuration is introduced, consisting of a magnetic field curvature $B_2 \neq 0$ which makes the axial potential acting over the electron dependent upon the cyclotron quantum number n_p, as represented in figure 2.22.b). Although the magnetic field needs to be homogeneous for the trapping, as mentioned in section 2.3, in the Geonium Chip this new *magnetic bottle* configuration of the magnetic field can be easily introduced in the same trap by changing the set of input currents of the source, which are described in section 3.4, thus changing from homogeneous field to magnetic bottle in less than a minute [58].

Therefore, if Δn_p microwave photons with a frequency close to the cyclotron frequency ω_p are absorbed by the electron, it increases the energy of the cyclotron motion in Δn_p quantums and, due to the described dependence of the axial potential, this jump perturbs the axial frequency by $\Delta n_p \Delta\omega_z$. Being the unperturbed axial frequency ω_z^0, the final axial frequency becomes $\omega_z = \omega_z^0 + \Delta n_p \Delta\omega_z$, where $\Delta\omega_z$ is [13]

$$\Delta\omega_z = \frac{q\hbar B_2}{m^2\omega_z^0}. \tag{2.56}$$

The jump in the axial frequency is shown in figure 2.22.a), followed by a spontaneous emission after a cyclotron radiative lifetime τ_s. In the case of [13], this radiative time is

$$\tau_s^{even}(y_0) = \frac{mcC}{2\pi q^2}\frac{1}{\left|E^{even}_{CPW}\right|^2} \tag{2.57}$$

and

$$\tau_s^{odd}(y_0) = \frac{mcC}{2\pi q^2} \frac{1}{|E_{CPW}^{odd}|^2}, \tag{2.58}$$

where the indexes even and odd refer to the two propagation modes supported by CPW lines, E_{CPW} is the electric field, c is the speed of light in vacuum and C is the capacitance of the CPW per unit length [13]. The expressions of the electric fields are given in appendix A and show that this field depends on the distance between the CPW and the electron y_0. Therefore, the cyclotron radiative lifetime depends strongly on this height.

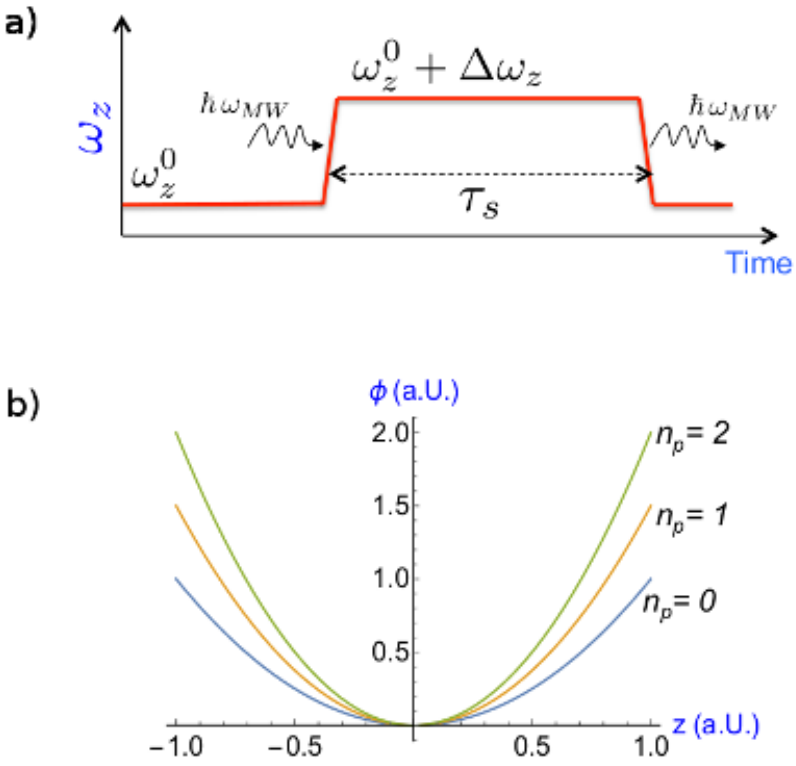


Fig. 2.22 a) Change in the axial frequency caused by the absorption of a microwave photon and spontaneous emission after a cyclotron radiative lifetime of τ_s. b) Different axial potentials as a function of the cyclotron quantum number n_p assuming $B_2 < 0$ [13].

A measurement of the axial frequency ω_z can be done in approximately 5 seconds with an accuracy of 1 Hz [13]. Although it is in the same order of magnitude as the quantum cyclotron radiative lifetime, as shown in figure 2.23, the detection of cyclotron quantum jumps requires only a measurement of frequency variations $\Delta\omega_z$. The latter can be measured considerably faster attending to its phase, as given by the following

expression [13]

$$\tau_m = \frac{\sigma(\Delta\phi)}{\Delta\omega_z}, \tag{2.59}$$

where $\sigma(\Delta\phi)$ is the minimum axial phase difference to distinguish between particles with cyclotron quantum numbers $n_p = 0$ and $n_p = 1$ [13]. According to the estimation of [13], a magnetic bottle in the Geonium Chip can be created such that it could reach $\Delta\omega_z = 1$ KHz, obtaining measurement times $\tau_m = 80$ µs, substantially smaller than the values of τ_s shown in figure 2.23. Thus, becoming possible the detection of cyclotron quantum jumps.

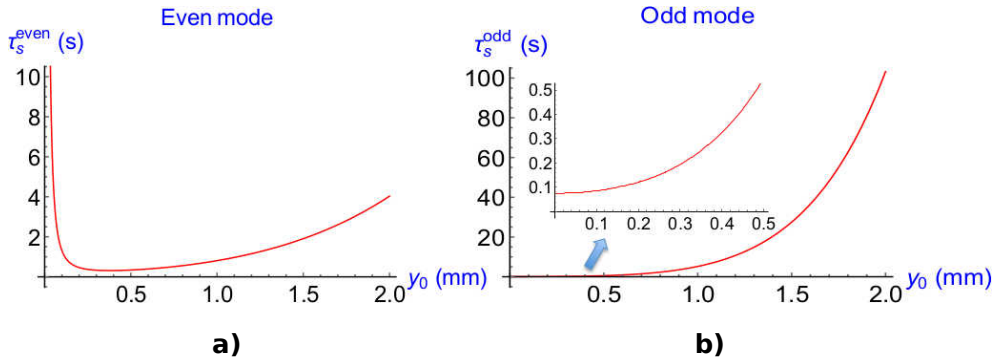


Fig. 2.23 Quantum cyclotron radiative lifetime for a)even and b)odd transmission modes of a CPW with the dimensions of the line presented in [13].

Chapter 3

Experimental set-up

In this chapter the mechanical design of the experiment components and the processes followed in order to fabricate it are described. It is not one of the main topics of the thesis, however the introduction provided here is essential to understand the experiment. Some of these experimental procedures have required several members of the team to be completed, therefore, although I have been involved in the development of most of these tasks, this work has been done in collaboration and based on the progress previously made by the rest of members of the Geounium Chip team.

The chapter includes a detailed explanation of the Geonium Chip inner cryogenic chamber preparation, which encloses the region where the electron would be trapped, the photoelectric effect used to eject electrons from the chamber and the trapping procedure, a introduction to the magnetic field source and the installation of a cooling system which helps to reduce the heat introduced in the experiment from external heat sources.

3.1 Inner cryogenic chamber

This section presents the inner cryogenic chamber currently used in the experiment, designed by J.Pinder, and the preparation for the trapping experiment. Although the design is the same that J.Pinder described in his doctoral thesis [75], some new improvements on the sealing and some new techniques developed to solve new problems are detailed in this chapter.

3.1.1 Design

The software chosen to design the inner cryogenic chamber is AutoCAD. The chamber of figure 3.1 was designed by J.Pinder [75] as a box made of conductor material to isolate the interior from any external electrical field.

Three holes are added: for the window, the pinch-off tube and the chip (Figure 3.2). The sealing of three of them is described in the next sections of this chapter.

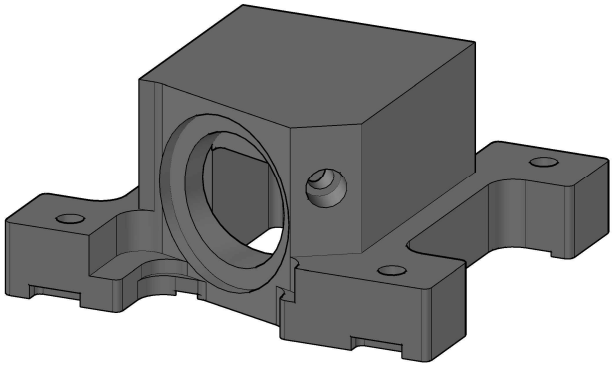


Fig. 3.1 Design of the inner cryogenic chamber designed by J.Pinder [75] in AutoCAD [77].

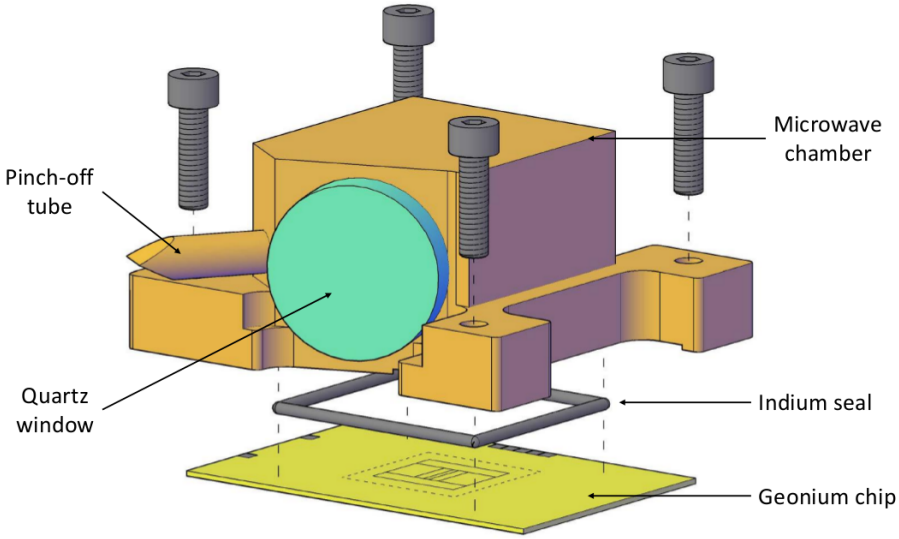
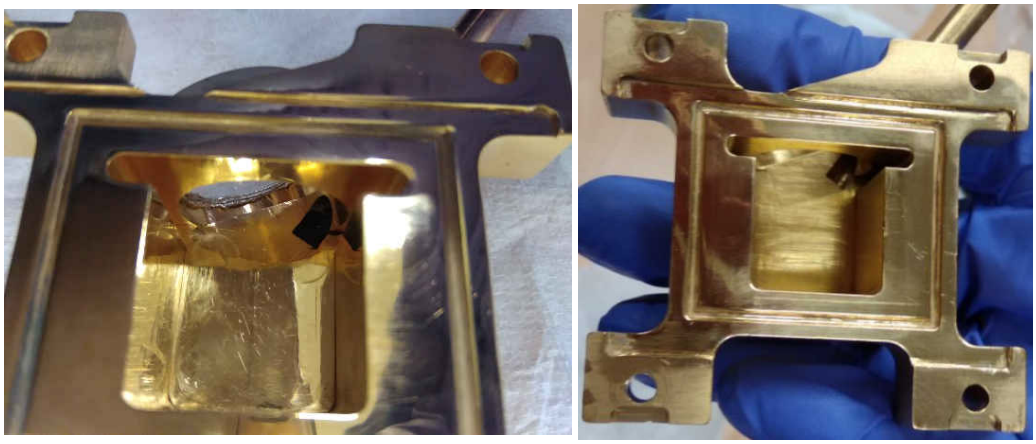


Fig. 3.2 Drawing of the inner cryogenic chamber with chip, window and pinch-off tube sealed [14].

The material of this new inner cryogenic chamber is oxygen-free copper (OFC), since it has better qualities for the thermalisation than the aluminium previously used.

3.1.2 Polishing the chamber

The internal walls of the chamber are polished in order to eliminate imperfections that can cause perturbations of the potential of the trap. A picture of a gold plated chamber with and without polishing can be seen in figure 3.3.



a) b)

Fig. 3.3 a) Polished inner cryogenic chamber; b) unpolished inner cryogenic chamber.

3.1.3 Gold plating the inner cryogenic chamber

First of all, cleaning the surface from any dirt, grease, oxide or any other residue is very important, since it ensures the correct reaction of the metallic wall of the chamber with the gold plating solution.

In order to protect the oxygen-free copper (OFC) of the chamber, the first step is polishing it, removing a layer of material. It can also be done chemically, with a solution of hydrochloric acid and water.

To remove dirt and grease the surface is cleaned with hot water around 50°C and soap. Additionally, a bath with ethanol or IPA (isopropyl alcohol) is applied to completely degrease the surface. Finally, the chamber is cleared with deionised water to completely remove any remaining residue.

The clean and polished chamber is submerged in a electroplate bath solution made by Gold Plate Services company, which gold-plates the OFC. Gold is very unreactive, so it is resistant to corrosion, maintaining the same electrical properties under exposure to air or other elements [75].

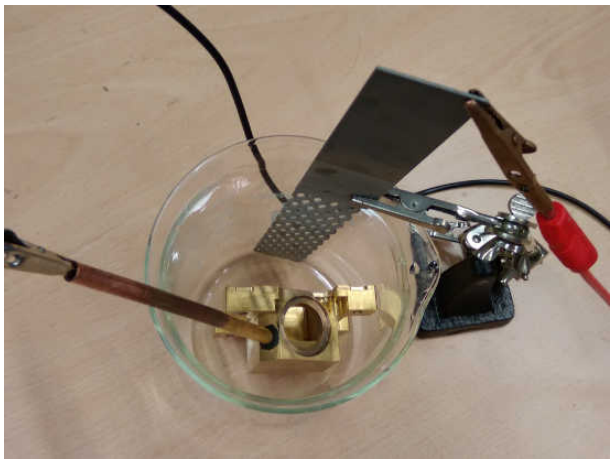


Fig. 3.4 Chamber in a vase with cathode, ready to gold plate.

3.1.4 The mesh

The chamber creates a conductive cavity with the surface of the chip, isolating the trapping region from external electromagnetic perturbations. However, The UV light of the loading procedure introduced in section 2.3, requires a hole and a window on one of the walls of the chamber, which could create a way for the electromagnetic noise to reach the interior of the cavity. To avoid this, a copper mesh is placed behind the quartz, covering the hole and in contact with the chamber, such that the UV light can pass through the mesh but it stops the external RF radiation.

The mesh is supplied by SPI Supplies. It has open area of 85% and a hole size equal to 234 µm.

It is held by a frame, which is soldered to the mesh with indium, as shown in figure 3.5. Both, the mesh and the frame, are made of copper and its shape is an square that will be placed on the hole made for the window on the chamber.

To remove any corrosion or oxide from the frame, sand paper and Scotchbrite pads are used. Next it is submerged in a solution of hydrochloric acid (figure 3.6) and water followed by a clearing with deionised water.

The next step is soldering the mesh as it appears in figure 3.7, using solder paste. Very small drops of solder paste are deposited over the copper frame and the copper mesh is placed over these drops. Finally, it is heated to solder mesh and frame together. After this procedure, the mesh with frame is submerged in a bath of hydrochloric acid and water again to remove the oxide due to the heating process and the exposure to air, and later cleared with deionised water.

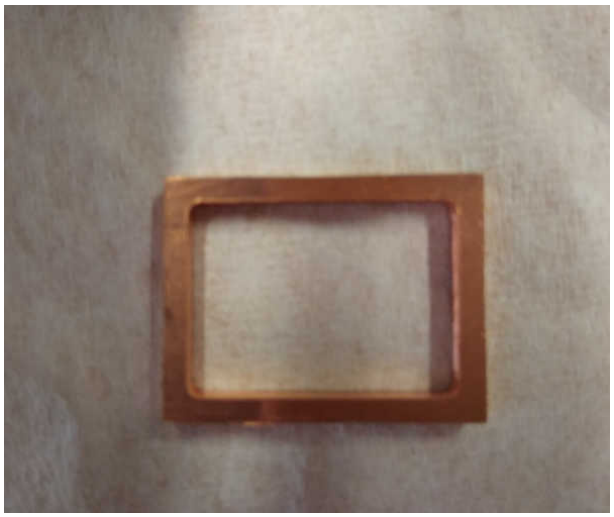


Fig. 3.5 Copper frame to place the mesh.

Fig. 3.6 Copper frame in hydrochloric acid and water solution.

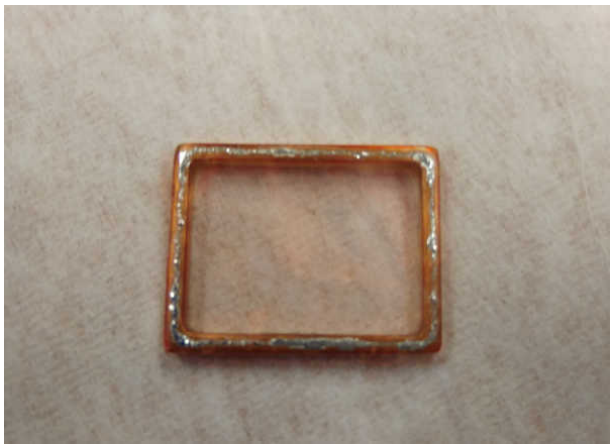


Fig. 3.7 Copper frame with copper mesh solder on the top.

Finally, trying to reduce the time of exposure to air in order to avoid corrosion or oxidation, the mesh is submerged in the gold-plating solution, following the same

electroplating procedure that was done for the aluminium chamber. In this case a special holder for the mesh was created, as it is a very delicate piece and could be damaged by a normal connection with crocodile clip. The holder is formed by a long screw connected to the voltage source and a piece of PCB where the mesh rests, ensuring the electrical connection between the screw and the mesh. A picture of the gold plating with the described tool is shown in figure 3.8 and the resulting gold plated mesh is in figure 3.9.

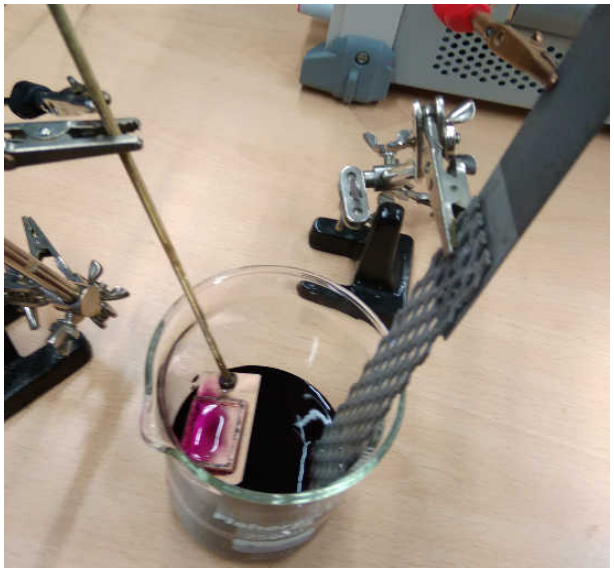


Fig. 3.8 Gold plating of the mesh.

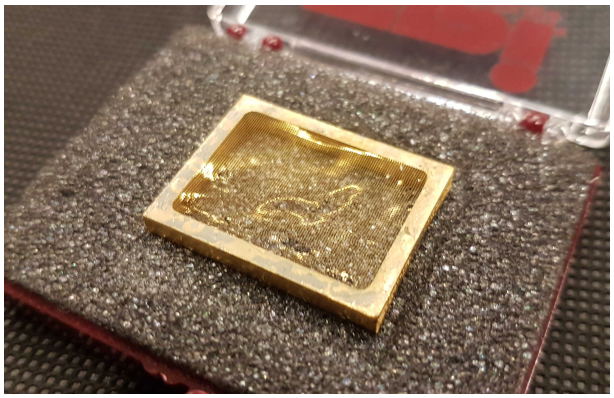


Fig. 3.9 Gold plated mesh and frame.

3.1.5 The pinch-off tube

The pinch-off tube 3.2 is a copper tube with a diameter of 6 mm, that is connected to the chamber in order to evacuate the air inside the chamber.

Although in previous versions the tube was stuck to the chamber with Epoxy, soldering it with indium has been found as the most reliable solution, as it is malleable and resists

better heating and cooling cycles. In order to make a good sealing, the surface of the chip and chamber needs to be clean of any dirt and corrosion. So, previous to the soldering process, the oxide is removed by using Scotchbrite pads and then it is cleaned with hot water and soap, cleared with ethanol or IPA and finally cleared with deionised water.

The pinch-off tube is cut with a special pinch-off tool, which applies pressure, sealing it and holding the vacuum at the same time that the cut is done. A picture of the pinch-off tube cutting and the final result can be observed in figures 3.10 and 3.11 respectively. This process was described with more detail in J.Pinder thesis [75].

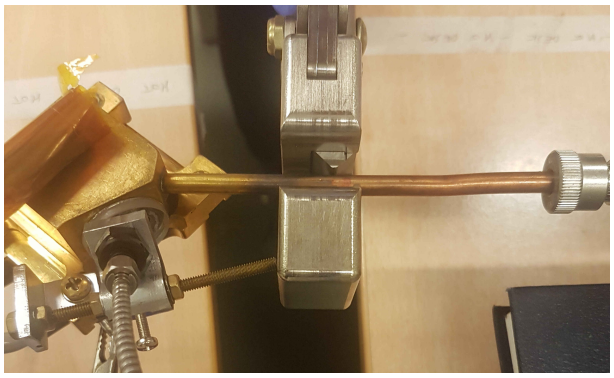


Fig. 3.10 Pinch-off process.

Fig. 3.11 Pinched-off tube.

3.1.6 Sealing the window

The window is a circular piece of quartz, which, as it was tested by J.Pinder [75], holds the vacuum inside the chamber, while the UV light can pass through.

To seal the window to the chamber, a layer of indium is soldered on the border of the window. After that, the indium is compressed, using compression aluminium plates (figure 3.12), getting a perfect planar indium seal over the border of the chamber and avoiding any irregularities over on the shape of the indium. Also, when it is compressed it spreads over the glass resulting in a better seal. Hence, it is perfectly sealed and no leaks can appear between the quartz and the indium.

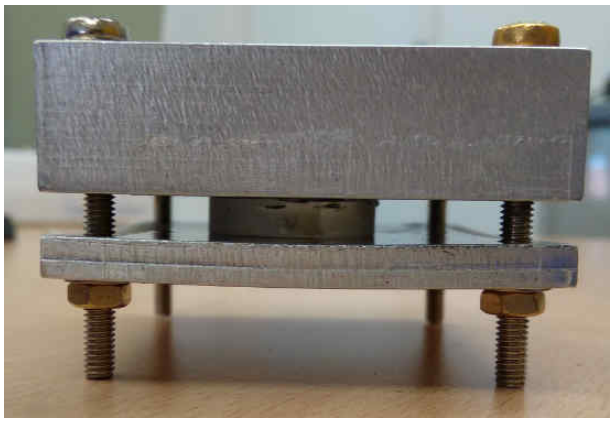


Fig. 3.12 Window with indium being compressed by the compression plates.

Although the final and optimal procedure to seal the window to the chamber, which is the one used currently in the experiment, involves only indium seals, the first attempts were made with Epoxy, as introduced in [75]. In this section both techniques are described.

Sealing the window to the chamber with indium and Epoxy

This technique of sealing the window and chamber with Epoxy was dismissed as presented problems, being damaged after several cooling-heating cycles. However it is described here since it was part of the work done during the thesis and can be of interest for future developments.

The indium is sealed to the gold-plated inner cryogenic chamber with Epoxy. The chamber needs to be completely clean previous to the sealing to ensure that the seal is as good as possible. Soap and hot water are used to clean it and ethanol to remove any possible residue. Then, the indium seal is covered by Epoxy and the window with the indium and Epoxy is placed over the chamber hole, which has been specially designed for this. It is important to check that the Epoxy covers all the perimeter of the glass, sealing it to the chamber. The window does not have contact with the Epoxy as it could break the quartz with changes of temperature due to different thermal expansion coefficients of the materials. Hence, the indium seal is between the Epoxy layer and the window, as it appears in figure 3.13. The elasticity of the indium will protect the quartz from the contraction of the walls of the chamber.

The Epoxy will need to cure at room temperature for 24h (figure 3.14), because heating it to accelerate the process could damage the indium seal.

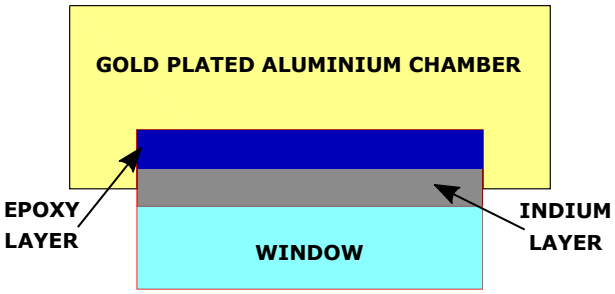


Fig. 3.13 Layers of indium and Epoxy between the chamber and the window.

Fig. 3.14 Curing the Epoxy layer between the chamber and the window.

Once it is totally cured, it is tested by using the vacuum pump and some ethanol over the seal. If any leak is detected in the Epoxy seal of the window, more Epoxy is applied over the leak using a syringe as in figure 3.15. The syringe is used to repair the leak very precisely and with the smallest amount of Epoxy in order to avoid contact between the Epoxy and the window, for the reasons explained above.

Attempt to reseal the window

After many cycles of heating the chamber, the Epoxy and indium seal of the window were damaged. The possible solutions were repairing the seal or resealing it again.

The first one could be faster, but it could not easily be done in our laboratory. The attempt to reseal the window was made by heating it to melt the indium and close the possible gaps or holes created in the sealing. As it can be observed in figure 3.16, the chamber will rest over the window while it is being heated, so the gravity will help to compress the window and the chamber, and to close the gaps. However, this process failed after several attempts. The reason could be the bad sealing of the indium or damage

Fig. 3.15 Syringe with epoxy to repair precisely the leaks of the window sealing.

on the Epoxy after many heating cycles and exposition to other chemical products, such as ethanol or acetone.

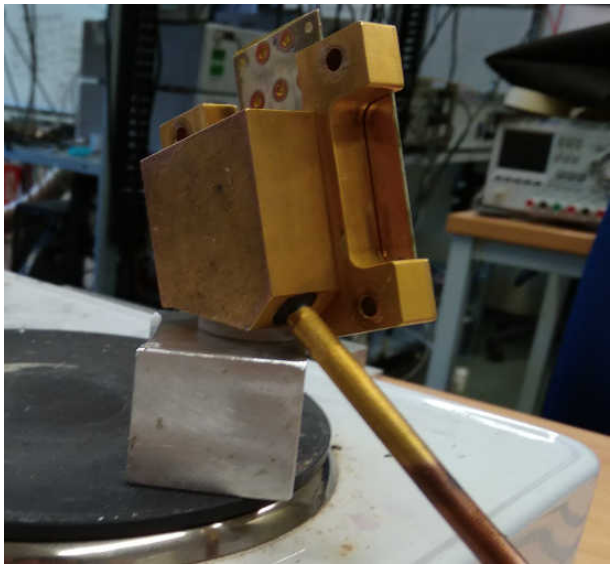


Fig. 3.16 Indium in the gap of the inner cryogenic chamber and ready to seal the chip to the chamber.

The second one takes more time as the window needs to be taken off, the indium seal melted, the surface cleaned and the sealing process repeated again. First the chip and mesh are removed from the chamber to avoid any damage. Then, the chamber is heated on the hot plate until the indium is melted and the window can easily be removed.

Sealing the window to the chamber with only indium

In this case the window will be sealed to the chamber using only indium (figure 3.17). Different techniques have been tested, all of which are described in this section.

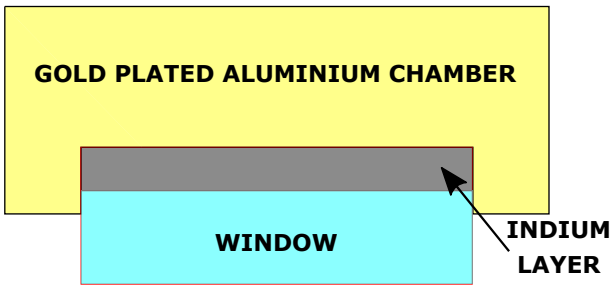


Fig. 3.17 Layer of indium between the chamber and the window.

The different techniques used in order to seal the chamber to the window only with indium use a combination of soldering and pressure methods. The soldering is made in a argon chamber, which avoids the oxidation of the indium during the soldering process. To pressure both together, window and chamber, two aluminium pieces are designed and that fit perfectly with the shape of the chamber, hence the pressure is applied evenly over every wall of the chamber. In order to protect the window, a piece of PTFE is placed between the window and the aluminium.

The two different techniques used are:

- Soldering the window to the chamber with indium:

  The first attempt was sealing the window to the chamber by soldering it with indium.

  The window is previously soldered with a flat layer of indium as described above. Then, a small layer of indium is placed over the chamber and the whole chamber is warmed up to the melting temperature of indium. Once it is reached, the window is carefully placed over the indium and the whole system is cooled down.

  The resulting sealing was not good enough as big leaks were detected when it was tested with the pump. An attempt of repairing it by pressing the window against the chamber and heating it (to make the indium more malleable) was made with no successful results. A picture of this repairing attempt can be observed in figure 3.18.

- Pressuring the window and the chamber: A layer of indium is soldered over the window and the chamber. The layer of soldered indium is made flat by cutting it as

Fig. 3.18 Window being pressured against the chamber in order to repair the indium seal.

flat as possible with the scalpel and pressuring it. By making it flat the contact of the indium of the window and the chamber at every point is ensured. Once both layer of indium are totally flat, they are cleaned with a solvent, such as ethanol, and pressured together. The pressure process is slow, since both indium layer need to seal. The indium shape has to be slowly readapted to the sealing in order to avoid damages on the window.

No leaks were detected by using this method.

3.1.7 Sealing to the chip

The sealing of the chamber to the chip requires totally clean and polished surfaces. The polishing is made by using the Dremel machine and very smooth tools. The surfaces of the chip and chamber are both polished and cleaned with hot water, soap and ethanol. A picture of the polished surface of the chamber can be observed in figure 3.19. Then, they are sealed using indium.

To seal the chip and the chamber, the indium is placed in between them, over the small groove created on the inner cryogenic chamber for this reason (figure 3.21). The indium wire used for the sealing needs to be cleaned with a solver such as ethanol before being used, in order to remove any grease or oxide that can appear. Then, it is compressed by using a compression plate with four screws. The indium will be compressed as the screws are tied. It is a very slow process as the indium takes time to fill every gap and we need to avoid any kind of pressure on the chip that can crack it. Once the screws are tied enough, the compression plate remains for some minutes compressing the indium until it

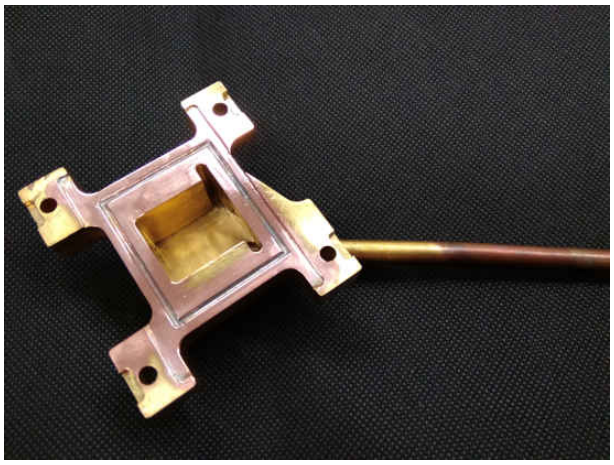


Fig. 3.19 Polished surface of the chamber ready to seal the chip.

get re-adapted to the new shape. Finally, the compression plate is removed and the chip is hermetically sealed to the chamber.

Removing the chip from the chamber

Whether the chip cracks or access to the inside of the chamber for any other reason is needed, such as changing the components inside, the chip needs to be taken off. In order to do this, heat is applied on the bottom of the chip, so the indium is melted and the chip is unsealed. This is a complex process as the chamber, the chip or the rest of the components can be damaged by the heat. It is necessary to be specially careful with the window and the chamber itself:

- Firstly, the window is sealed using the same material, indium, and it also could be melted and unsealed in the process of melting the indium on the chip. To avoid that, the chip is removed as soon as the indium is melted, so the temperature gradient in the copper chamber keeps the temperature of the indium seal of the window slightly lower, since the window is further from the heat source than the chip. Hence, the indium seal of the window will not be melted while the indium seal of the chip is. However, after many cycles, the sealing of the window could be damaged and it needs to be remade (see subsection 3.1.6).

- The chamber could be oxidized due to high temperature. This can be avoided by reducing the time of heating the chamber and doing the process very carefully, keeping the temperature as low as we need to melt indium, but not higher than that.

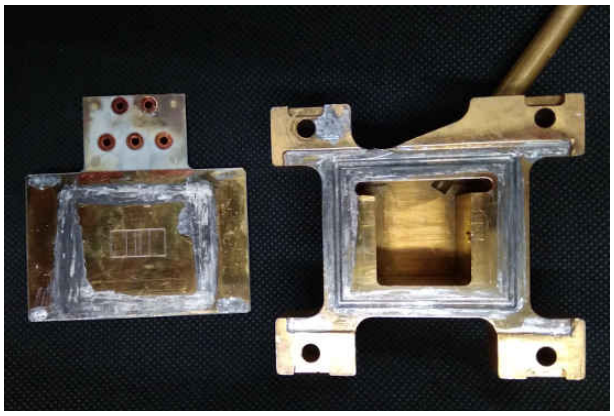


Fig. 3.20 Cryogenic chamber and chip taken apart by melting the indium seal.

Also, some indium residues could remain on the chamber, as it is not possible to remove all of them completely without polishing the chamber again. The polishing removes the indium and the layer of gold. Hence, once the polishing is done, the copper surface will need to be gold-plated again.

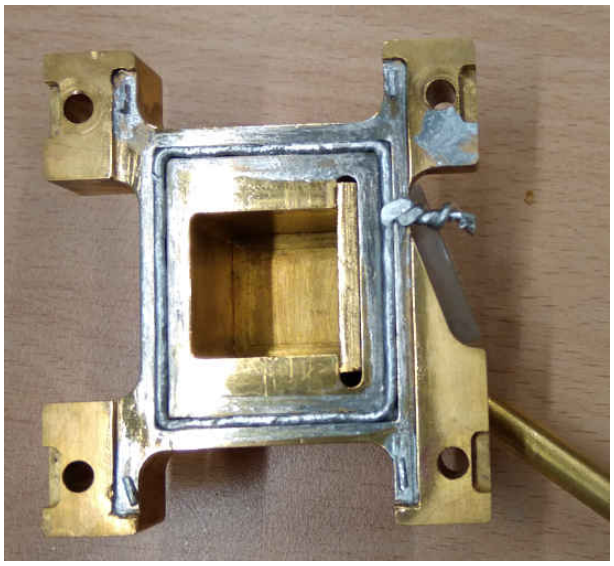


Fig. 3.21 Indium in the groove of the inner cryogenic chamber ready to seal the chip to the chamber.

3.2 Photoelectric effect

The photoelectric effect is used during the loading procedure, described in section 2.3, as a method of ejecting electrons from the surface of the inner cryogenic chamber [75]. UV Light with a wavelength in the range of 200 - 1600 nm is generated by a 9 W tungsten halogen lamp in a *Hamamatsu* UV source, transmitted by a optic fibre pointing through

the window of section 3.1.6 and applied over a wall of the chamber, generating a cloud of electrons.

The level of the photocurrent is a crucial element to consider during the trapping, as it is directly related to the amount of electrons that reach the trapping region and, therefore, the probability of success in the trapping. In this section, some changes in the set-up and some new procedures are described in order to increase the photocurrent level.

3.2.1 Targets

The targets are small pieces of different materials that will release electrons more efficiently than the wall of the chamber. Different targets are tested, in order to find the more effective one. The target is stuck inside the chamber in a place that can be reached by the UV light coming from the window, as it is shown in figure 3.22.

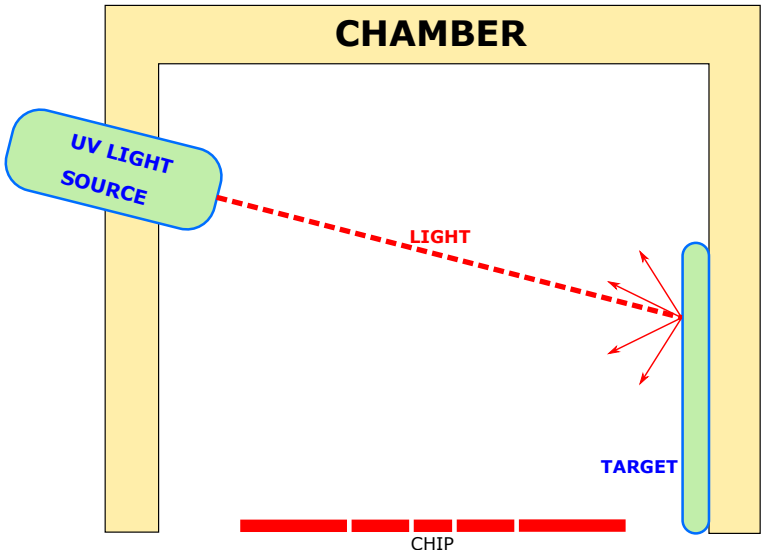


Fig. 3.22 Target inside of the chamber.

Goldplated copper with holes

This target is a gold plated copper layer with holes, manufactured in our laboratory. To create this target, a tool from a Dremel machine is rolled over a copper layer (figure 3.23), creating some holes on it. The layer with holes is gold plated to avoid corrosion on the copper.

The light has multiple reflections due to the holes and it increases the amount of electrons released by the photoelectric effect. It is easy to understand with figure 3.24.

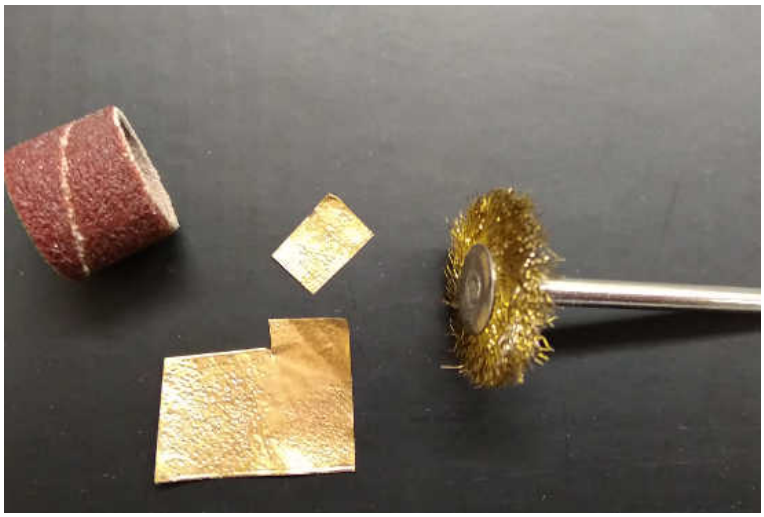


Fig. 3.23 Target manufacturing.

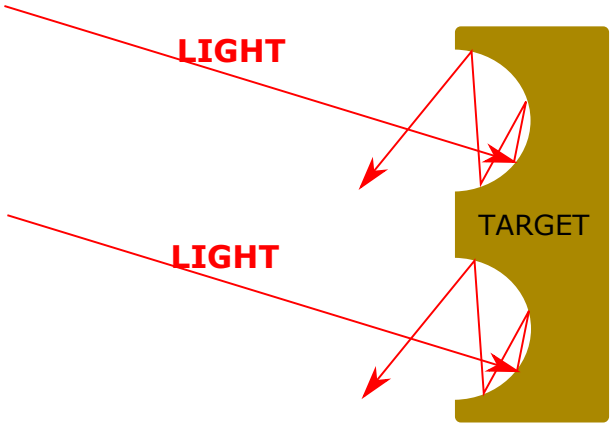


Fig. 3.24 UV light reflections in the holes created on the target.

Gold leaf

In order to stick the gold leaf over the Cryogenic chamber wall, the gold leaf with the paper attached, as it is supplied by the seller, is placed over a few drops of deionized water on the wall of the chamber. As the paper gets wet, it unsticks the gold leaf. The paper can be removed very carefully by using the pliers and the gold leaf remains floating on the water. Then, once the deionized water is dried, the gold leaf stays over the gold layer of the chamber wall and remains attached to it (figure 3.25).

Final results of the photocurrent measurements with different targets

A more exhaustive research of this topic has been done by R. Willetts, including more measurements of different materials, and it has been concluded that the gold leaf is the

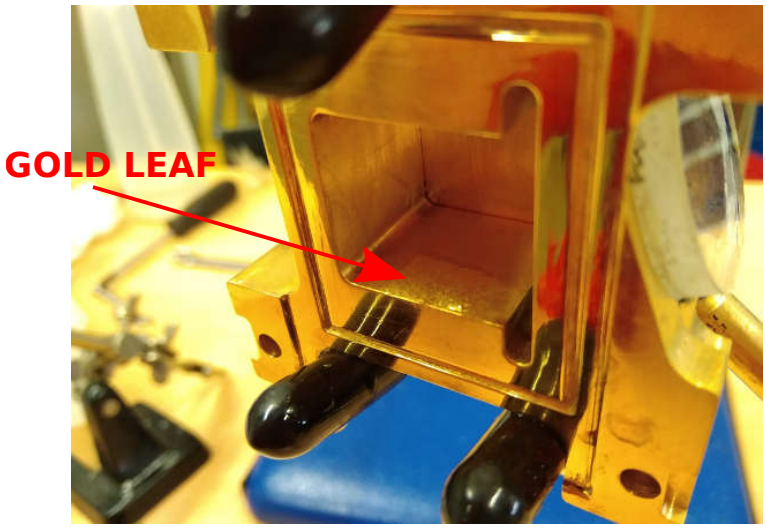


Fig. 3.25 Target inside of the chamber.

best of the evaluated targets, generating a 48% higher current than silver paste, which is the second best result.

The material of the target is gold, with a work function of Φ_{AU} = 5.1 eV [75, 72] and the energy of the UV light with 240 nm is hf = 5.17 eV. Therefore, according to equation 2.38, the temperature of the trapped electrons before being cooled is [75]

$$T_{electron} = \frac{hf - \Phi}{k_B} = \frac{(5.17eV - 5.1eV)\,e}{k_B} = 812K. \tag{3.1}$$

3.2.2 Baking the chamber

To accelerate the out-gassing processes in the chamber, it is heated up to 105°C. In this section the set-up and the process followed to bake the chamber are described.

A DHT052020LD heat tape and two *Rohde & Schwarz HMP4040* power suppliers connected in series are used to increase the temperature of the chamber. Firstly, the chamber is covered with aluminium foil (figure 3.26) to homogenise the distribution of the heat during the heating process. Secondly, The tape is placed over this aluminium foil as it appears in figure 3.27 and is then covered with aluminium foil again to homogenise the temperature over the whole piece (figure 3.28). Finally, the chamber is connected to the pump and, to hold it, a common clamp protected from the heat with Kapton tape is used, as shown in figure 3.30.

While the chamber is being heated, the out-gassing is removed by the pump. During this process, the chamber sealing, described in section 3.1, could be easily damaged by

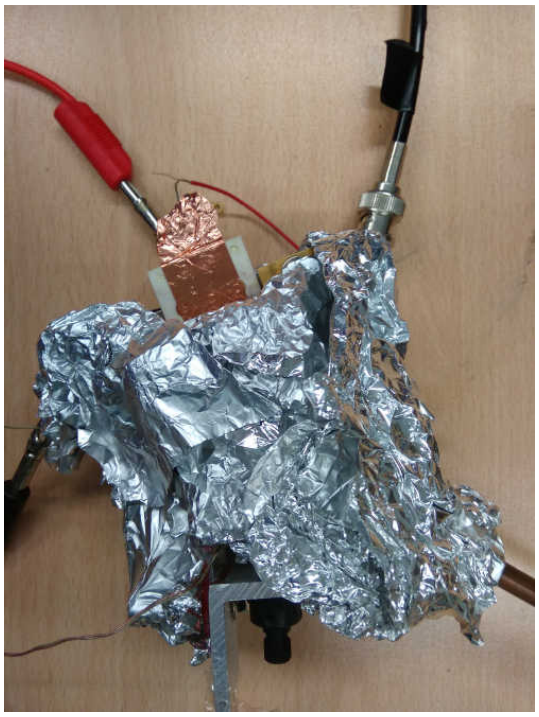


Fig. 3.26 Cryogenic chamber covered by aluminium foil.

Fig. 3.27 Heat tape over the cryogenic chamber.

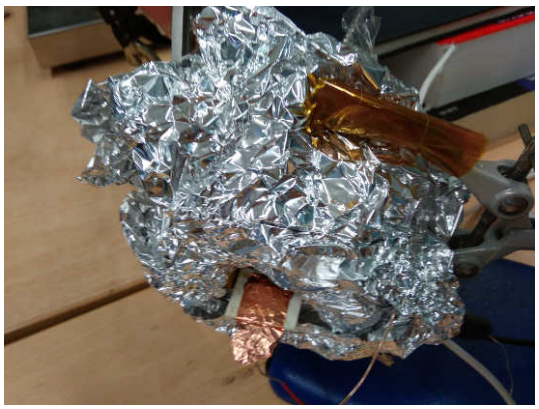


Fig. 3.28 Cryogenic chamber and heat tape covered with aluminium foil.

the thermal expansion-compression cycles. This is a delicate process that needs to be monitored all the time, which is done with a LabVIEW program created by Ryan Willetts.

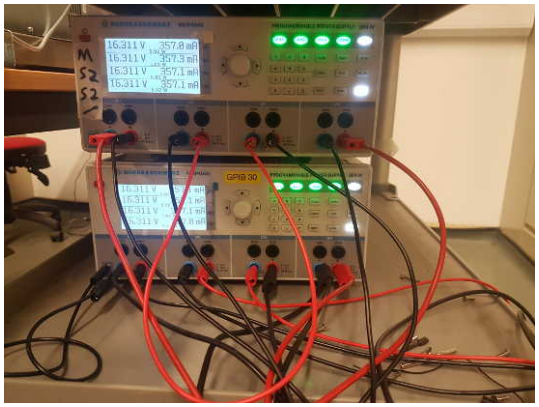


Fig. 3.29 Heating tape power source working to keep the system at 100°*C*.

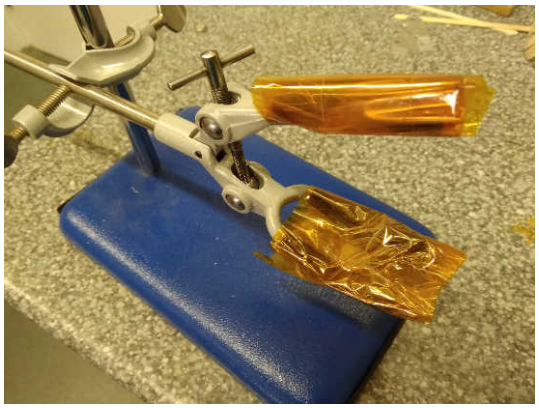


Fig. 3.30 Clamp covered with kapton tape.

3.2.3 Wiring set-up for the measurements

The electrodes of the chip are connected to a *Rohde & Schwarz HMP4040* power source that supplies 32 V, while the rest of the chip and the chamber are grounded. It will attract the electrons released by the photoelectric effect. Thus, the picoammeter is able to measure the generated photocurrent. This set-up can be observed in the schematic of figure 3.31.

3.2.4 Photocurrent measurements

The devices are controlled with a LabVIEW program developed by Ryan Willetts, which switches the UV source on and off several times, calculating an average value of the photocurrent with the time.

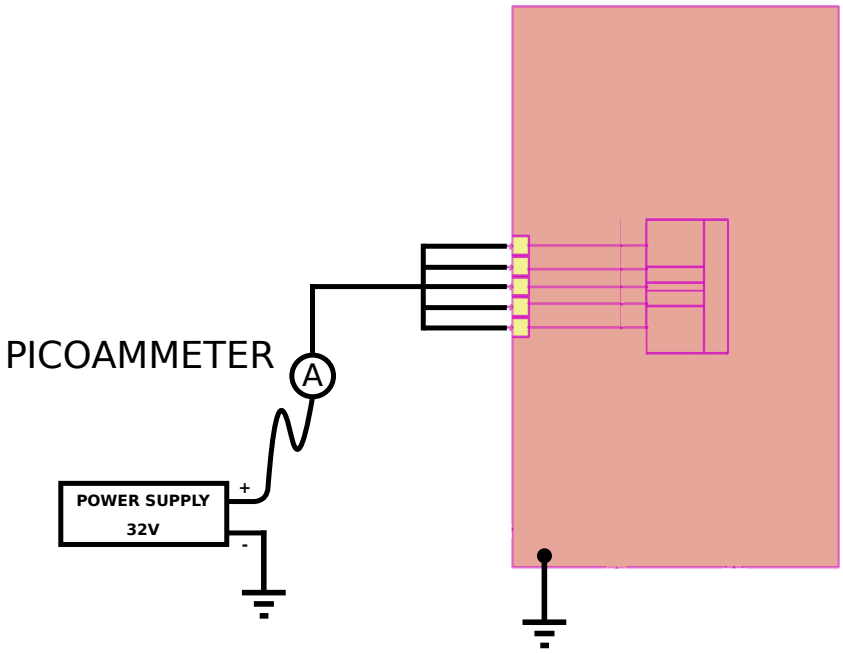


Fig. 3.31 Wiring to measure the photo-current.

This section shows a comparison of the photocurrent measurements in the inner cryogenic chamber before and after the baking out process. The same chamber was measured after baking out using the same set-up and the same equipment. The data of the measured pothocurrent in both cases are listed in table 3.1, where an increment of 4.63% can be detected after baking out. The data obtained are represented in the graphs of figure 3.32.a) for the case before and in figure 3.32.b) for the case after the baking out process.

Set-up	Photocurrent (pA)	Error (pA)
Before baking out	83.6	0.6
After baking out	471	2

Table 3.1 Photocurrent measurements before and after baking out the inner cryogenic chamber.

3.3 Loading procedure and rise time of electrical filters

The loading procedure consists of a combination of adiabatic and sudden changes in the potential of the trap electrodes in order to capture the electrons with enough energy to reach the trapping region. This was programmed with LabVIEW by R. Willetts, controlling two different voltage sources: *Time Electronics 5018 Multifunction Voltage Calibrators*, which supplies a very precise and stable voltage, and *Tektronix AFG3101*, that can increase the

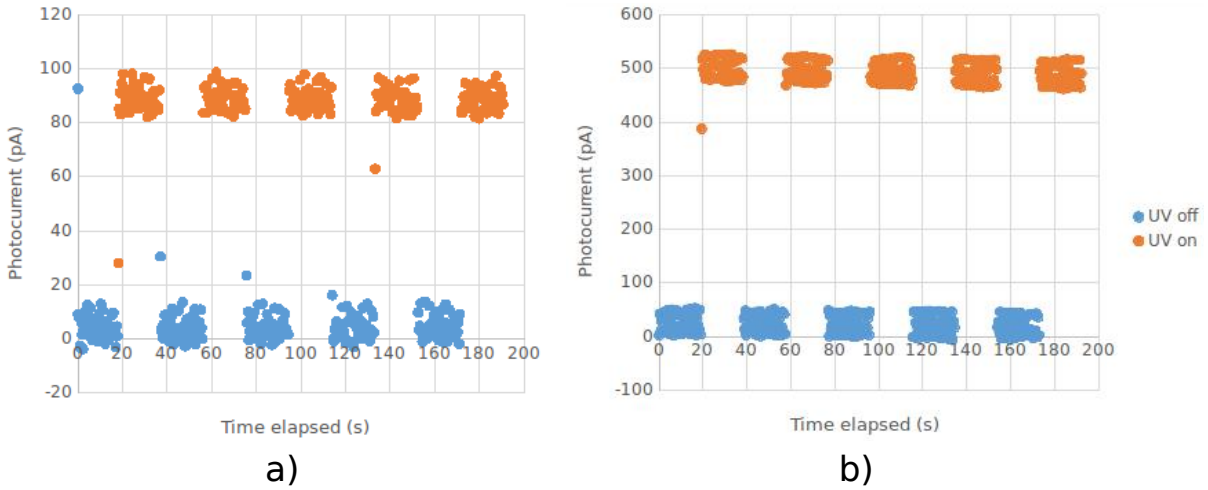


Fig. 3.32 Photocurrent measured in the inner cryogenic chamber with a) no previous baking out process b) after baking out.

output voltage with a short rise time in order to trap the electrons that have penetrated to the trapping region.

This rise time must be considered, since it can prevent the procedure to trap the electrons. Hence, not only the rise time of the voltage source has to be measured, but also the delay introduced by the rest of the components of the system. In this case, the limiting factor is the delay produced by the filters. The measurements of the delay of the filters are presented in this section.

3.3.1 Loading procedure

The electrons are ejected by UV light with photoelectric effect, as introduced in sections 2.3 and 3.2, from a target placed over one of the walls of the chamber, as shown in section 3.2.1.

As it can be observed in figure 3.22, this target is closer to the Correction and End-cap electrodes of one side of the trap, which was described in section 2.2. Considering this, the potential of the trap at the beginning of the trapping procedure, while the electrons are being ejected, is asymmetrical: the potential applied to the End-cap and Correction electrodes closer to the target is lower than the potential applied to the Correction and End-cap electrodes of the opposite side of the trap. Therefore, the electrons are ejected closer to the electrodes with lower potential and they can penetrate into the trap through this lower potential region. However, they can not scape trough the opposite side of the trap as the potential is higher. Once the electrons are in the trap, it needs to be closed,

that means, a sudden rising of the lower potentials, becoming it a symmetrical trap and capturing the electrons before they can bounce and leave trough the lower potential region. This procedure has been represented by Ryan Willetts in figure 3.33, where the lower potential region closer to the target is represented with the negative values of the Z axis.

The Tektronix source is used for the steps described in this paragraph, since it has a short rise time, smaller than the bounce time of the electrons.

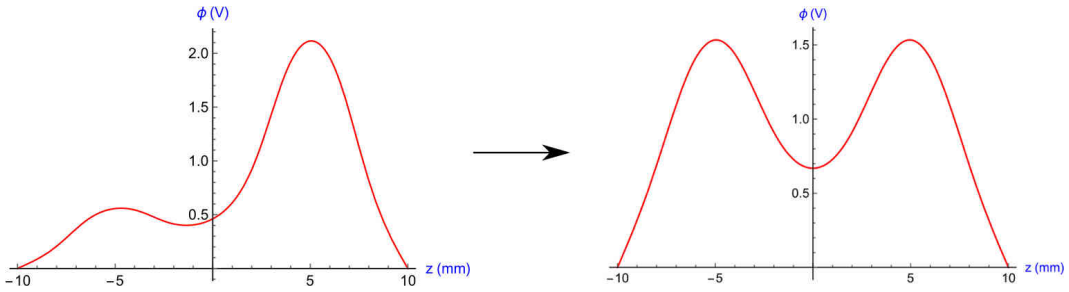


Fig. 3.33 Rising of the trap voltages during the loading procedure.

After the electrons are trapped, the voltages of the electrodes are changed adiabatically in order to create a symmetrical and harmonic potential and optimize the tuning ratio, as explained in section 2. At this point the trapped electrons could be detected. The Time Electronics voltage sources are used for this part of the procedure, as they are very stable and avoid any fluctuation in the voltages that can shift the frequency of detection.

In order to change from the Tektronix voltage source, used for trapping, to the Time Electronic, two switched are included. Therefore, once the trapping has concluded, the Time Electronic is connected and then the Tektronic is disconnected, supplying a voltage to the electrodes at all times.

3.3.2 Electrical filters

Three stages of filters are introduced in the connection between the electrodes of the Geonium Chip and each power supplier, such that most of the noise of the potential applied to the electrodes can be removed. The filters, designed by April Cridland [14], are lowpass RC filters formed by a 100 kΩ resistor and a 100 pF capacitor in series, as shown in figure 3.37.

Although the filters are necessary to avoid any noise in the electrodes, the delay introduced in the rise time of the voltage applied to the electrodes can impede the loading of the trap, which requires sudden changes of this potential. Therefore, every filter has

two Schottky diodes placed in different directions, which allow the signals with higher amplitudes than the Schottky diodes threshold to bypass the filters, while the noised is filtered.

A measurement of the final delay in the rise time of the signal is necessary to determine whether the trapping signal applied to the system is able to trap electrons. In this section the delay introduced by the filters is measured, firstly using a prototype, which has been measured at room temperature and in liquid nitrogen to analyse the variation in the threshold voltage of the Schottky diodes with the temperature, and secondly measuring the rise time of the filters installed in the main experiment.

Filters board prototype

A prototype of the filters system is created in order to analyse the shift of the threshold voltage in the Schottky diodes at very low temperatures, which could affect to the final rise time of the voltage applied to the electrodes.

The prototype is made with the same type of wire that is used in the real experiment and with a similar length. There are three stages of filters, separating the first one by a flange to simulate the real conditions of the cryostat. A schematic of the prototype set-up is shown in figure 3.34 and a picture of the real prototype is in figure 3.35.

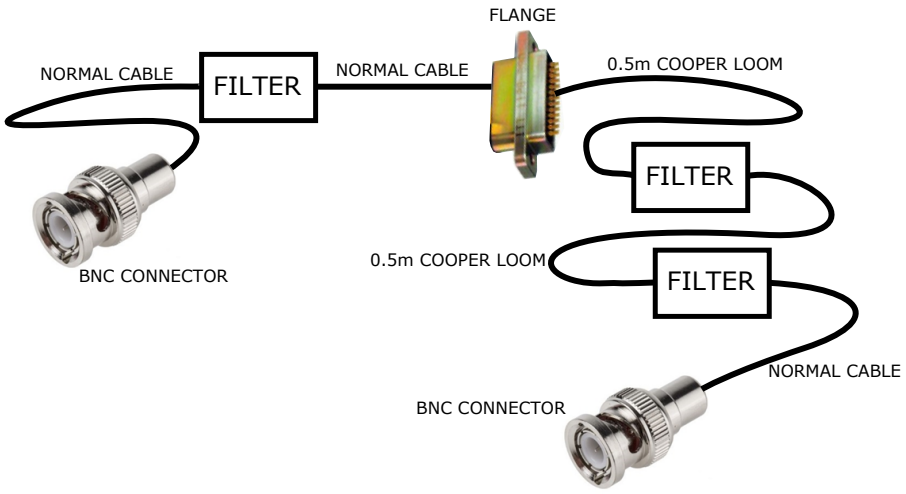


Fig. 3.34 Schematic of the filters prototype set-up.

The amplitude of the signal at the output as a function of the amplitude at the input shows the threshold of the Schottky diodes, which, depending on the temperature, is between 3 V and 4 V. It is measured at room temperature and with the prototype in liquid nitrogen and the results are in figure 3.36

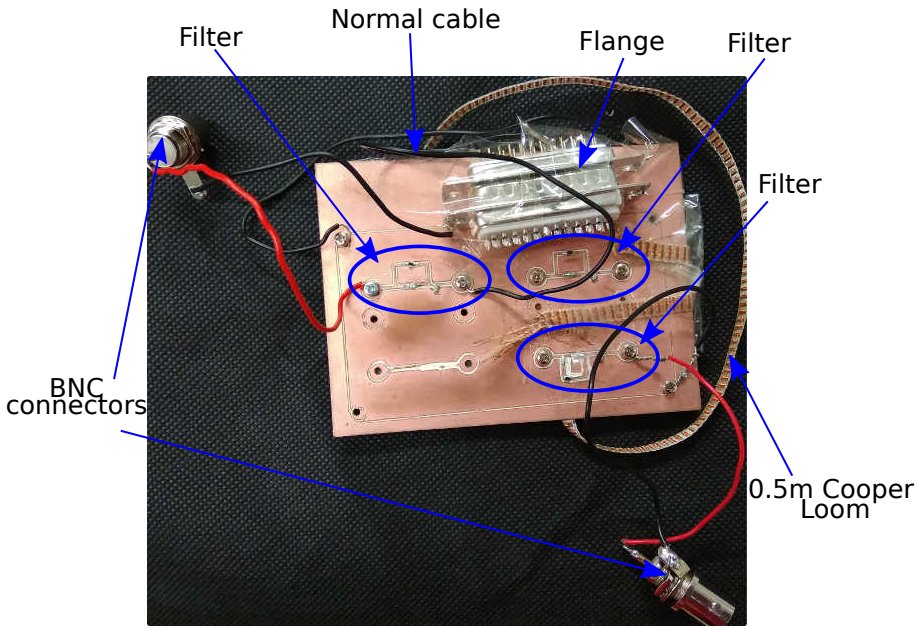


Fig. 3.35 Filters prototype picture.

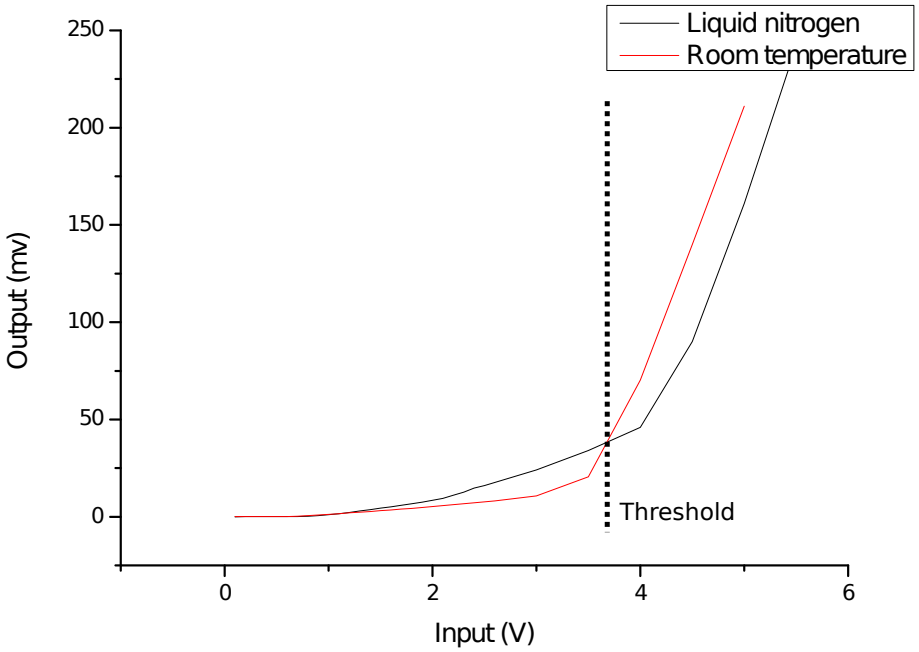


Fig. 3.36 Experimetal measurement of the threshold of the prototype diodes at different temperatures.

Measurement of filters in the main experiment

The delay in the rise time of a signal caused by the filters is measured by applying a signal at the input of the filters and using as output a new cable connected to the left End-cap electrode of the chip in the cryostat. The complete set-up is shown in figure 3.37.

To ensure a good thermalisation through the new cable used for the measurements, the material of the added cable is steel, with a low thermal conductivity. In addition,

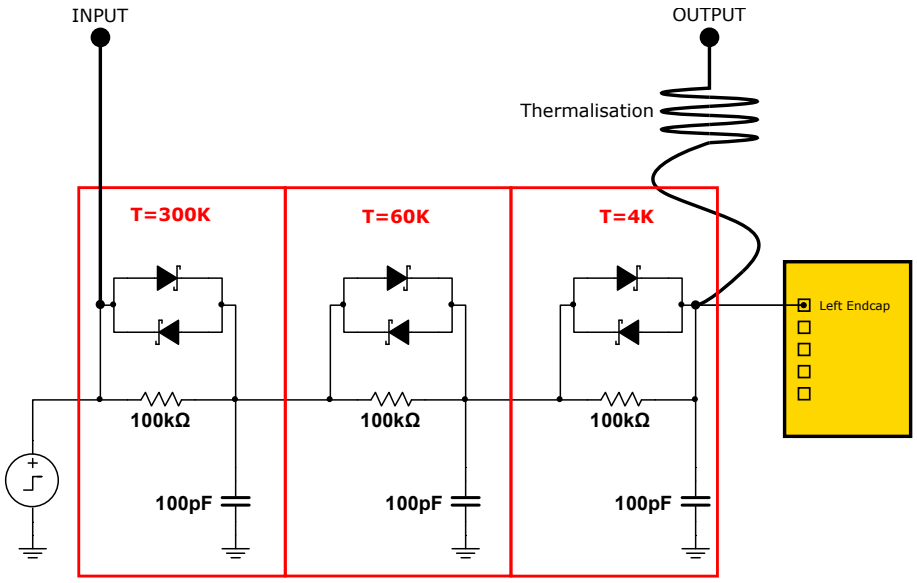


Fig. 3.37 Rise time filters measurement set-up.

the coplanar waveguide (CPW) line of figure 3.38 is connected to this cable in order to improve the thermalisation.

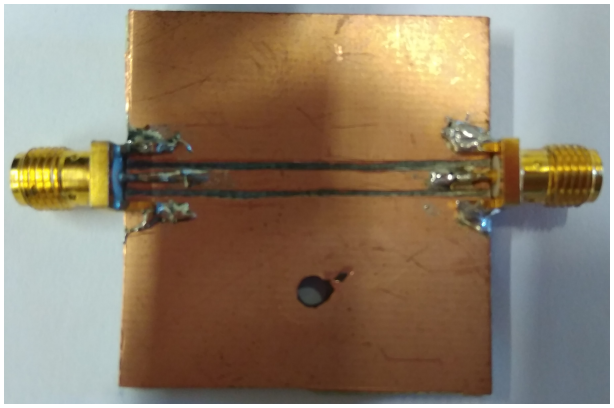


Fig. 3.38 CPW for thermalisation.

The graph of figure 3.39 represents the measurement of the amplitude at the output vs the amplitude at the input of the filters at 4 K. The threshold is approximately 5 V at 4 K.

The final measurements, shown for different temperatures in figures 3.40 and 3.41, prove that the signal bypasses the filters through the Schottky diodes and the rise time affected by the delay of the filters is considerably short, thus the system could be used for trapping of electrons.

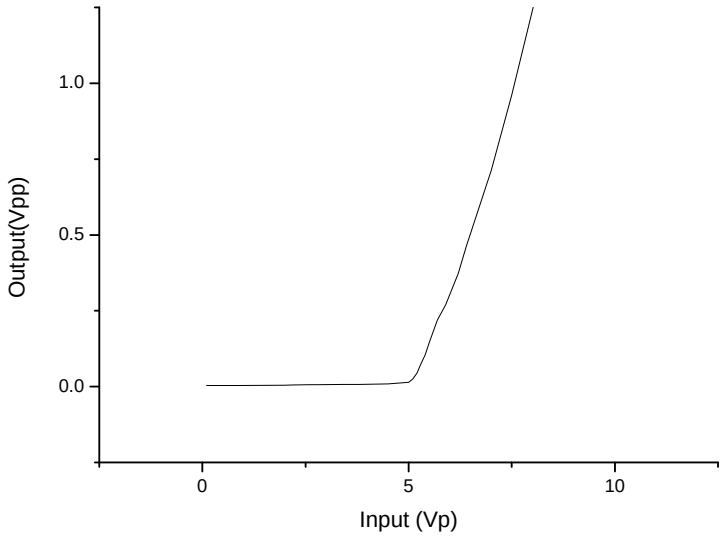


Fig. 3.39 Threshold of the diodes at 4 K.

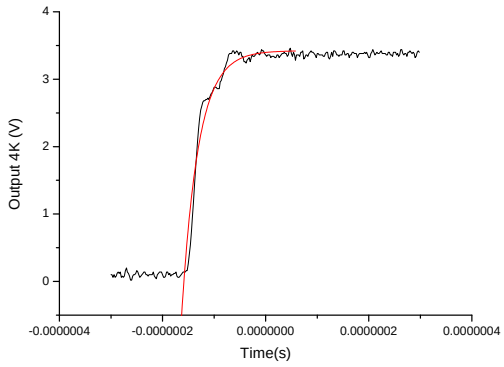


Fig. 3.40 The time constant of the rise time measurement at 4 K is 32.42 ns.

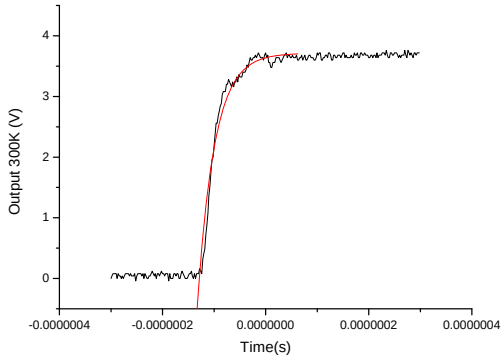


Fig. 3.41 The time constant of the rise time measurement at 300 K is 33.06 ns.

3.4 Magnetic field source

The magnetic field source consists of eight superconducting coils that generate a magnetic field which confine the electron as described in section 2.2. A new magnetic field source model is being developed by our team. In this new design, the magnetic field would be created by persistent currents and controlled with a flux pumping method invented by J.Lacy [58, 59]. However, it is still being developed and, therefore, this section describes the source model used currently in the experiment, created by J.Pinder [75].

The magnetic field source is composed of four pairs of symmetrical coils, as shown in figure 3.42: Main Wire, Shim 1, Shim 2 and Shim 3. Four of them are fixed to an aluminium case as observed in figure 3.43. Finally, it is placed underneath the trap, touching the bottom of the chip, with the centre of the source under the centre of the Ring electrode.

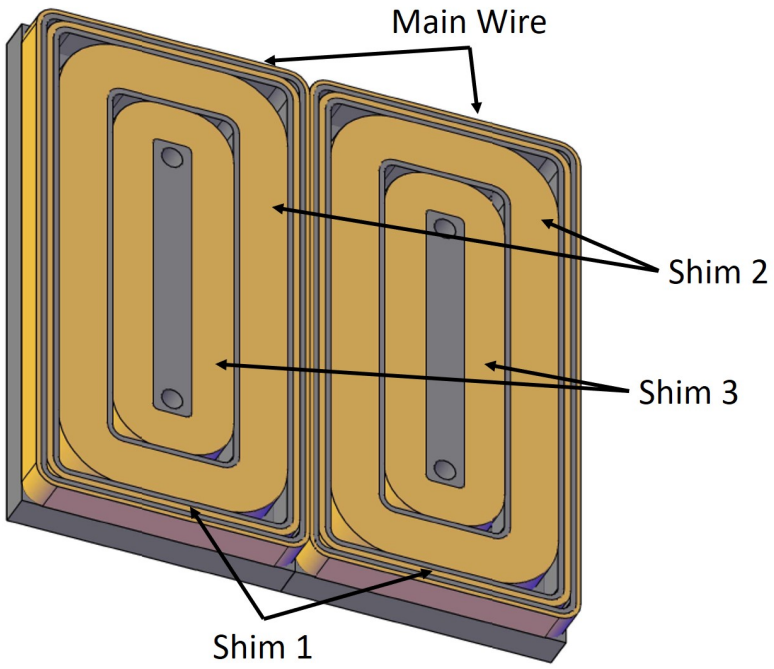


Fig. 3.42 CAD of the magnetic field source with the name of the four different coils [14].

Although the structure of the source currently used in the experiment is similar to the one described previously in [75, 14, 58], some changes have been done in order to create a stronger magnetic field with lower currents. The new wire used has a thickness of 100 µm, while the wire of the previous source was 400 µm. Hence, as it is thinner than before, it is possible to increase the number of turns of wire, increasing as well the magnetic field generated by this source with no increment of current. The number of turns in every

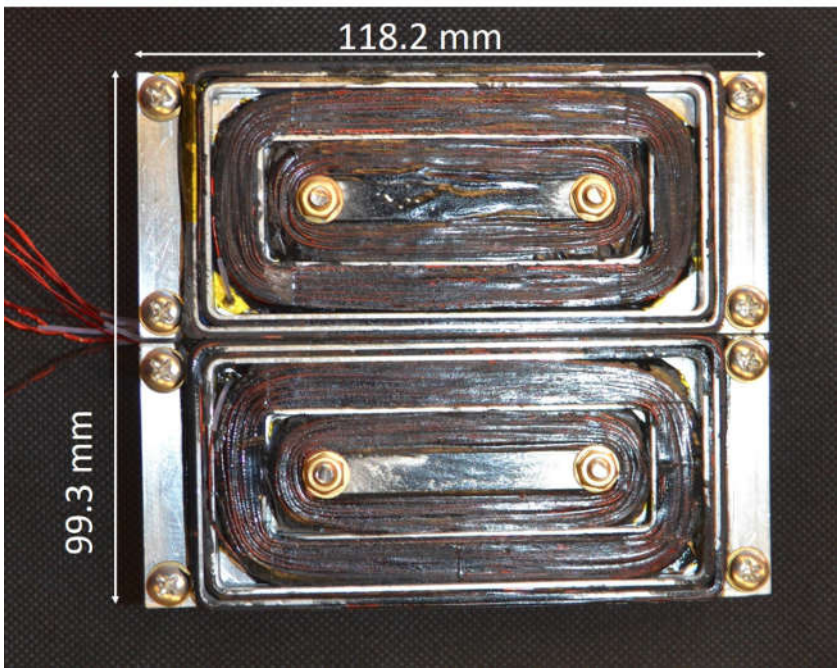


Fig. 3.43 Photo of the magnetic field source [14].

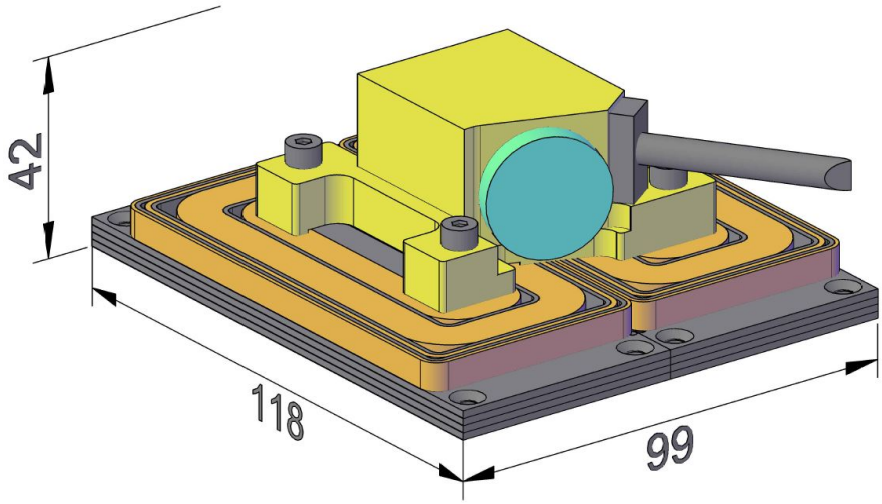


Fig. 3.44 Position of the magnetic field source under the chip and the inner cryogenic chamber [14].

coil, which is calculated to generate a homogeneous magnetic field over the trapping region, is 125 for the main and 233, 1976 and 1787 for shim 1, 2 and 3 respectively. Each coil is connected to one of the four power suppliers Rohde & Schwarz HMP4040 and the homogeneous magnetic field created by them is calibrated as a function of these currents as described in [14].

A homogeneous field of 0.5 T generated by the new source has been measured at the trapping position, although lower fields will be used to trap to avoid the risks of 'quenching'.

3.5 Cooling system

The high currents used by the magnetic field source described in section 3.4 increase the temperature of the system, outside and inside of the cryostat. It is a problem for the cryostat as it can not keep the temperature inside as low as it is required, but also, since the temperature reaches very high values, the system outside can be damaged. To avoid this risk, a cooling system is installed. This section provides a description of the combination of air-cooling and water-cooling techniques, which has been designed focusing on the reduction of the noise added by this new cooling system to the experiment.

3.5.1 Air cooling system

The air cooling system was designed by J.Pinder in order to keep as low as possible the temperature of an aluminium box that contains the filters for biasing the axial amplifier [14, 75] and the cables for the magnetic field source [58, 14, 75]. This box is physically connected to one of the flanges, that means, it is the last stage before the cryostat, hence, removing the heat introduce through this connection is essential. It consists of the fan shown in figure 3.45, that cools the box from the bottom, and the metallic mesh of figure 3.46 on the top, which allows the air to flow while isolates the system from external noise.

3.5.2 Water cooling components

The water cooling system keeps the electric devices of the cooling system, such as pump or fans that could potentially add electrical noise, separated from the experiment. Hence, the water absorbs heat from the heat source while the cooling system removes heat from the water in a separate place, avoiding any noise source to be in touch with the experiment.

The cooling system is composed of a pump with a water reservoir, a radiator, four fans, four water blocks and the tubing with connectors:

- Pump: the model is XSPC D5 Photon 270. The maximum flow of this pump is 1200 lph and it has a reservoir with a capacity of 690 ml [101].

Fig. 3.45 Fan of the filter box. Part of the air cooling system.

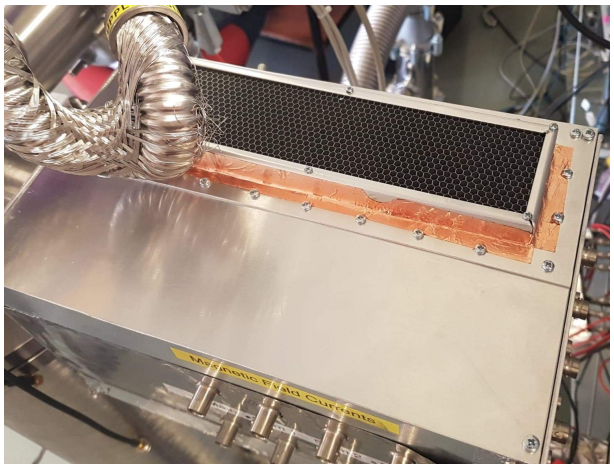


Fig. 3.46 Mesh of the filter box. Part of the air cooling system.

- Radiator: The radiator model is EX480 Quad Fan. At this stage, in order to remove the heat from the water, it flows through a very narrow metallic structure with four fans. The dimension of the radiator are 121x35.5x515 mm and it is made of Copper and Brass [102].

- Fans: Four fans Game Max Mistral32X are connected to the radiator. The speed of these fans is 1300 RPM and the dimensions 12x12 cm [65]. Although this could be one of the main sources of electrical noise of the cooling system, it is electrically isolated from the experiment.

- Water blocks: The water blocks model is NEXXXOS XP3 LIGHT, which is specially designed for PC processor; however, the size and characteristics fit with the requirements

of our system. The dimensions are 63x73x15 mm. It has two parts: a cavity, which allows the water to flow inside, made of PMMA and a smaller copper surface, which allows thermal conductivity between an external hot system and the fluid flowing inside [37]. The water blocks are placed on the top of the resistor at the input of the cryostat, as these are the main heat sources (more details in section 3.5.3). They are held by a small L-shape holder manufactured in our laboratory (Figure 3.48). In addition, thermal paste is applied to ensure the contact of the water blocks with the resistors, increasing the contact area as much as possible.

- The tubing is a hose of polyurethane with 10 mm of external diameter and 8 mm internal [35].
- The connectors: they are G1/4" made of brass. Elbow connectors [96] will be used to connect the water blocks with the tubing and two easy release connectors [36] are installed between the rest of the cooling system and the water blocks, which allows to connect and disconnect the water blocks from the rest of the water cooling system easily with no water losses.
- Biocide: This liquid biocide with 2.15% of Benzalkonium chloride is a liquid added to the distilled water to avoid any micro-organism growing inside that could be problematic as they increase the conductivity of the water of the circuit [61].

3.5.3 Water cooling set-up

The water cooling set-up is shown in figure 3.47. The water blocks are connected in series using the elbow connectors and tubing described in section 3.5.2, as it appears in figures 3.53 and 3.49, so water flows throw all of the water blocks placed over the resistors, removing the heat from them. The water blocks are held by the small aluminium brackets of figure 3.48, manufactured in our laboratory using a *High-Z CNC table* machine. Two easy release connectors are used, as described in figure 3.47 in order to disconnect the cryogenic system from the rest of the cooling system.

To ensure the maximum transmission of heat from the resistor to the water blocks, thermal pasted is applied between them (figure 3.52).

Finally, the water absorbs the heat and transport it to the radiator, where the water circulates through very small pipes surrounded by dissipaters and four fans attached. So, the heat is dissipated and the water is pumped to start the cycle again (figure 3.47).

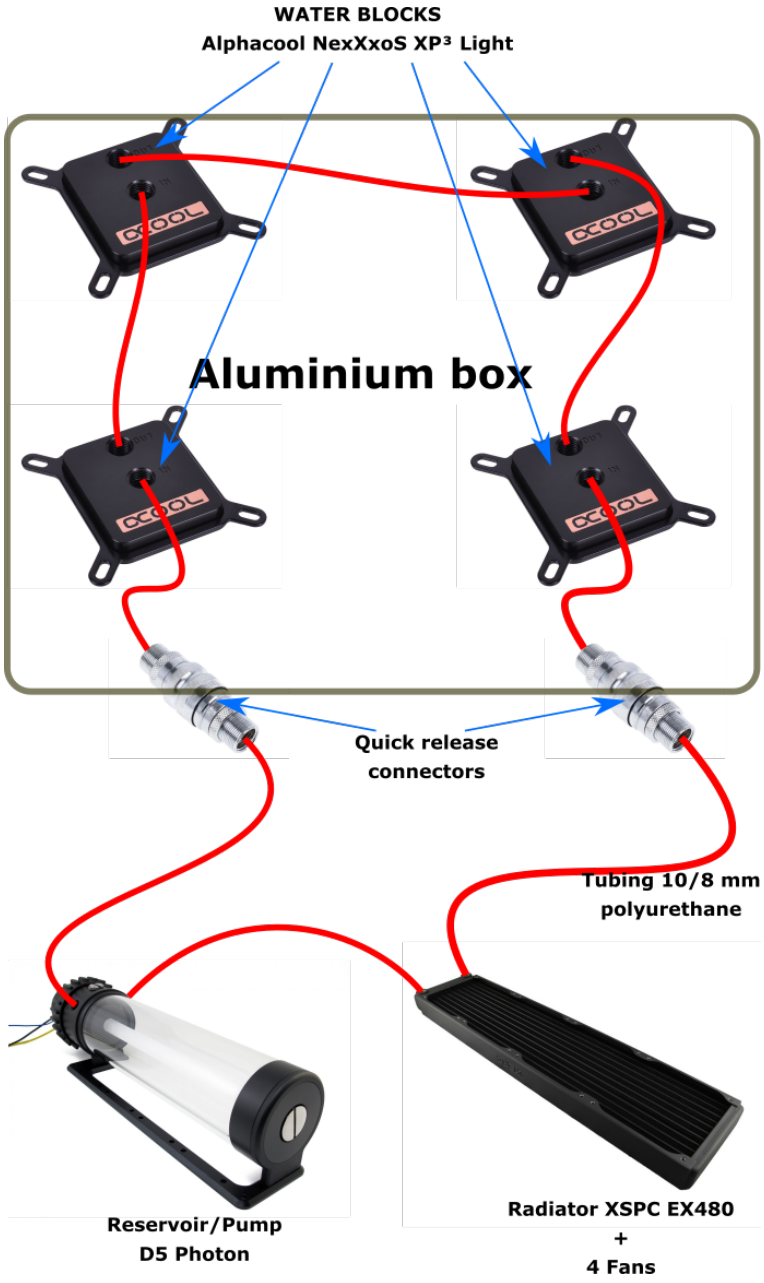


Fig. 3.47 Water cooling set-up.

3.5.4 Cooling system conclusion

The designed cooling system considerably reduces the heat in the cryostat and solves the previous problems related to overheating it. Also, it did not introduce electrical noise as the water cooling devices are electrically separated from the rest of the trapping system.

Fig. 3.48 Bracket to hold the water block.

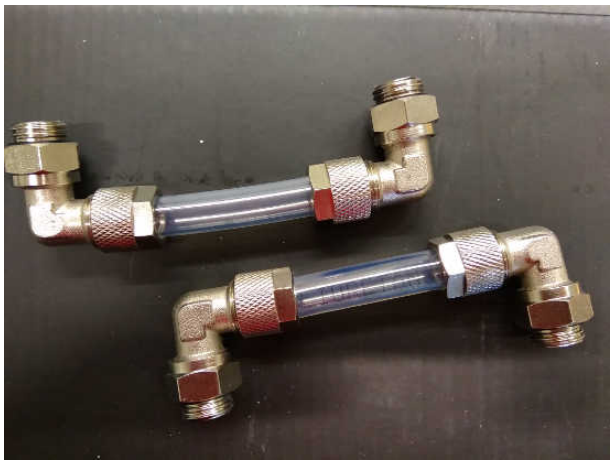


Fig. 3.49 Water cooling tubing.

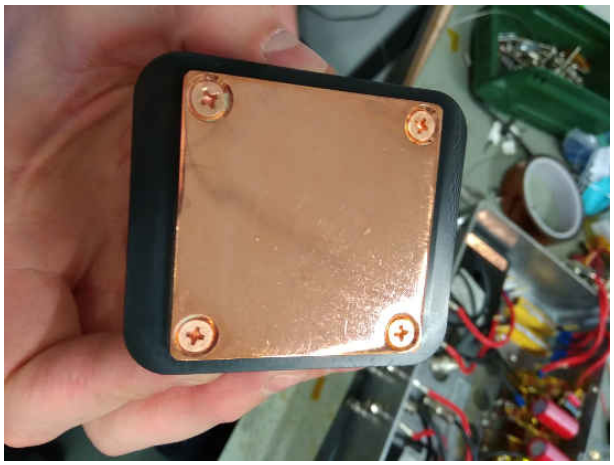


Fig. 3.50 Water block bottom surface.

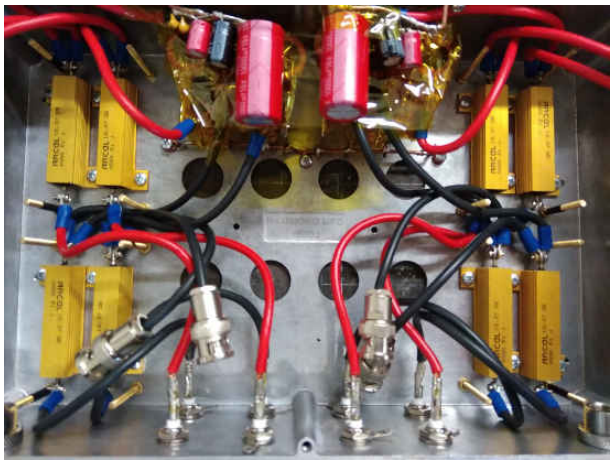


Fig. 3.51 Filters in the box before water cooling was installed. The water blocks are placed on the top of the resistors.

Fig. 3.52 Thermal paste over the resistors. The water block is placed on these resistors, hence the thermal paste helps the heat to be transmitted from the resistor to the water block.

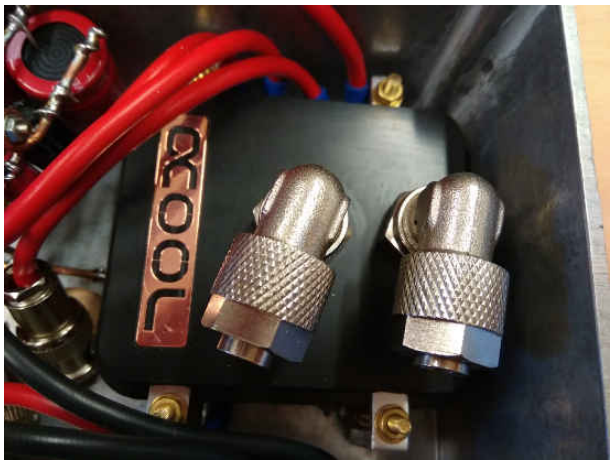


Fig. 3.53 Water block placed in the system over the resistors.

Chapter 4

High frequency properties of the Geonium Chip

The detection of the trapped electrons in the Geonium Chip can be perturbed if the capacitive or resistive effects of the chip are too high. Therefore, an in-depth study of the high frequency properties of the trap is essential in order to design a detection system able to detect these particles.

Two different models of the chip are analysed. The first one is a microfabricated chip described previously in [75] that was dismissed since the measurements showed in this chapter conclude that is not useful in our experiment. The second one is a PCB chip designed by J.Pinder. This last one is being used currently in the experiment.

In this chapter, these two models of Geonium Chip are analysed as high frequency devices. The S-parameters of the chip are measured with a *Keysight N9923A Fieldfox* Vector Network Analyser (VNA), transformed and analysed in order to get a complete description of the performance of the trap at high frequencies. The results of the investigation provide a detailed description of these characteristics and clarify the main problems to consider for the design of the chip.

Finally, the schematics of the chip were made with Advanced Design System (ADS), a software produced by Keysight EEsof and used for simulations of high frequency systems.

4.1 The capacitance problem

According to the description of section 2.6, the trapped ion is visible as a dip over the resonance of a superconducting coil (figure 2.20). This could be represented, as shown in figure 2.19, with a series resonator for the ion and a parallel resonator for the coil.

However, since it is a real implementation, the parasite elements of every component of the system must be considered. The influence of the parasitic capacitance added to the resonator is specially important because it could shift or destroy the resonance and the detection system would become useless. The components connected to the resonator which add capacitance are the amplifier and the chip, that could be analysed, attending to their electrical properties, as it appears in figure 4.1. In this figure, C_{chip} is the element associated to the chip, C_{in} and R_{in} are the input capacitance and resistance of the amplifier, the capacitor C_{ion} and inductor L_{ion} represent the equivalent circuit modelling the trapped ion, already discussed in section 2.6, and the components in the resonator box C_1, C_2 and L represent the equivalent circuit of the resonator.

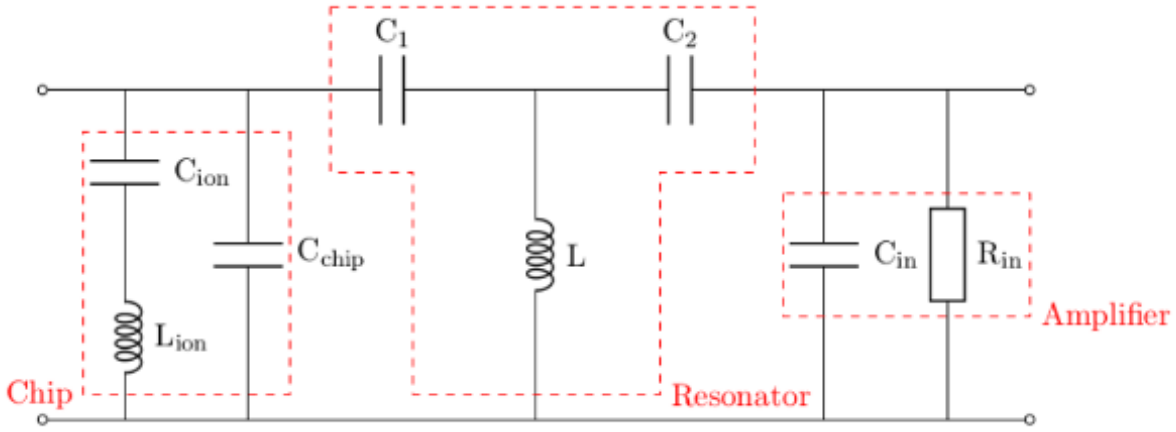


Fig. 4.1 Equivalent circuit of the trapped ion, chip, resonator and amplifier [14].

The components C_{chip}, C_{in} and R_{in} are not considered in section 2.6 as they are not ideal components, but parasites appearing from the actual devices used in the experiment. The effect of the amplifier is discussed in section 5.2, so this chapter focusses exclusively on the analysis of the chip.

The design of the resonator and the measurement of the quality factor described in section 5.1.1 and in [75, 14], are estimated for an unloaded resonator. However, considering

a resonator loaded by these parasitic components described above, the value of the quality factor deteriorates following the equation [92, 63]

$$Q_{expt.} = \sqrt{\frac{\omega_{expt.}}{\omega_0}} Q_0, \tag{4.1}$$

where Q_0 and ω_0 are the quality factor and the resonance frequency of the unloaded resonator and $Q_{expt.}$ and $\omega_{expt.}$ the quality factor and resonance frequency of the loaded resonator respectively [14, 92, 63]. Considering the capacitance C_{chip} described above, the value of this last frequency is given by the following equation

$$\omega_{expt.} = \frac{1}{\sqrt{\left(C_{chip} + C_{coil}\right) L_{coil}}}, \tag{4.2}$$

where C_{coil} and L_{coil} are the capacitance and inductance of the superconducting resonator described in section 5.1.1. Thus, the detection of the trapped particle could not be possible with the decrement of the Q factor due to the added capacitance and described in equation 4.1. Hence the high frequency properties of the chip, investigated in this chapter, must be considered in order to design a system able to show the dip created by the trapped ions over the resonance, following the explanation of section 2.6.

4.2 Fitting of impedances and admittances

In next sections, different set-up for the measurements are presented. The measurements are done with the VNA in order to obtain the S parameters, which represent the ratio of transmission and reflection of the wave from the ports where the measurement is taken. These are converted to admittance Y or impedance Z parameters, following the expressions given in appendix B.2.3, and analysed with the Π and T networks models described in section B.2.4, in order to determine the value of the high frequency parasitic components. A more detailed explanation of the analysis done in this particular case is provided below, whilst a complete introduction to the high frequency analysis and the S, Y and Z parameters can be found in appendix B.

4.2.1 Modelling the chip

The gaps between electrodes and between electrodes and Ground Plane are modelled following the equivalent circuit of the real capacitor described in [6] and shown in figure 4.2. For high values of R_p, which is the case of the chips analysed in this thesis, the model of figure 4.2 is similar to the circuit of a series resonator described in [77]. Therefore, the resonant peaks that appear in the measurement of impedance and admittance parameters of the chip are fitted with the expression of impedance and admittance of the circuit of figure 4.2 respectively, obtaining the values of capacitance C, inductance L and resistance R_s and R_p.

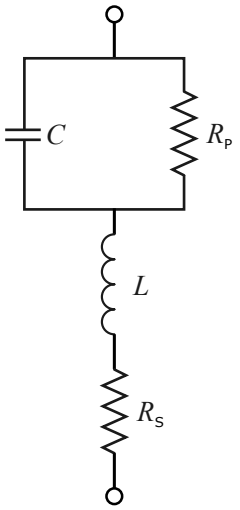


Fig. 4.2 Electrical model for Z and Y blocks. It is the equivalent circuit of a real capacitor [6].

To identify the effect of the capacitive effect of every component of the chip in the measured parameters, the Π and T networks models are used.

In the case of the admittance parameters, according to the introduction of appendix B, since this is a reciprocal system, that means, $Y_{21} = Y_{12}$, it can be analysed as the Π network of figure B.5.a), where $Y_{coupling} = |Y_{12}|$, $Y_{in} = Y_{11} + Y_{12}$ and $Y_{out} = Y_{22} + Y_{12}$.

The Π network configuration to measure the chip using the VNA is shown in figure 4.3. Each port of the VNA is connected to a different chip electrode while the rest of the electrodes and the Ground Plane are connected to GND. Hence, similar to the description of [83, 79, 10, 67] for the case of a CPW line, the $Y_{coupling}$ gives the coupling admittance between both electrodes, Y_{in} the admittance between the 'electrode 1' and GND and Y_{out},

between the 'electrode 2' and GND. The peaks of these three Y parameters are fitted with the model of the real capacitor of figure 4.2.

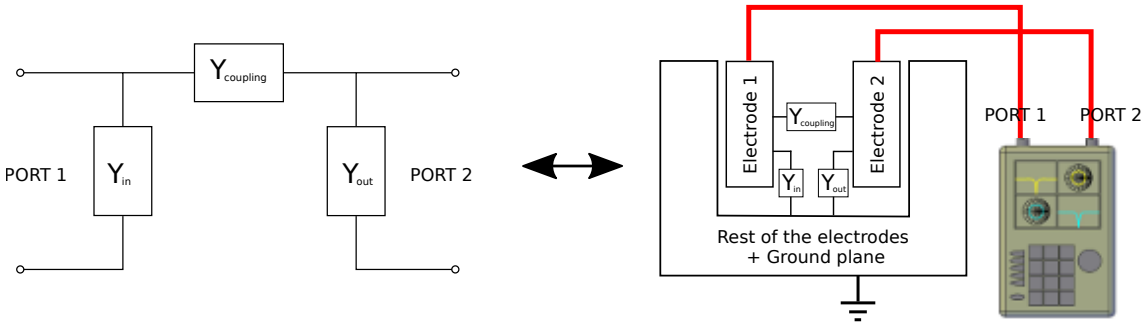


Fig. 4.3 Y parameters π network. $Y_{coupling}$, Y_{in} and Y_{out} are fitted with the admittance of the real capacitor model shown in figure 4.2.

Equally, the model of figure B.5.b) can be followed to measure the Z parameters. The configuration for the measurements of the Z parameters of the chip following the T network is shown in figure 4.4. For this configuration both VNA ports are connected to one particular electrode of the chip and the rest of electrodes and the Ground Plane are connected to GND, so Z_{12} is the total capacitance between the electrode connected to the VNA and the rest of the chip. Hence, the other two capacitances, $Z_{11} - Z_{12}$ and $Z_{22} - Z_{12}$, are equal to zero.

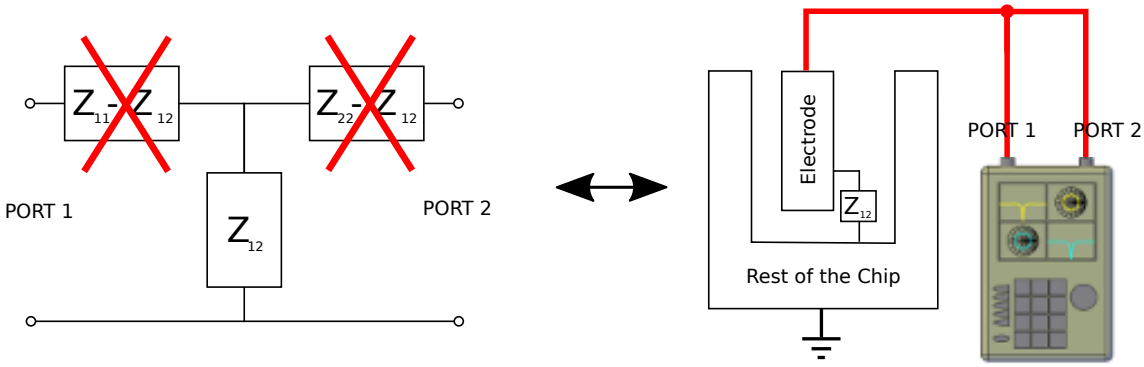


Fig. 4.4 Z parameters T network. Z_{12} is fitted with the impedance of the real capacitor model shown in figure 4.2.

4.2.2 *Pi* network set-up for measurements

The S parameters of the chip for every couple of electrodes are measured by connecting the VNA to these particular electrodes and grounding the rest of the chip, as seen in figure 4.3. Also, in order to get a stable ground, the grounded electrodes are connected to the electrical earth. Figure 4.5 shows the wiring diagram for the case of measuring the

Upper End-cap and Correction electrodes, with the rest of the electrodes and Ground Plane grounded. Although the model of circuit used for the representation of figure 4.5 is the MIR chip, introduced in section 4.3, the configuration is similar for any version of the chip characterised.

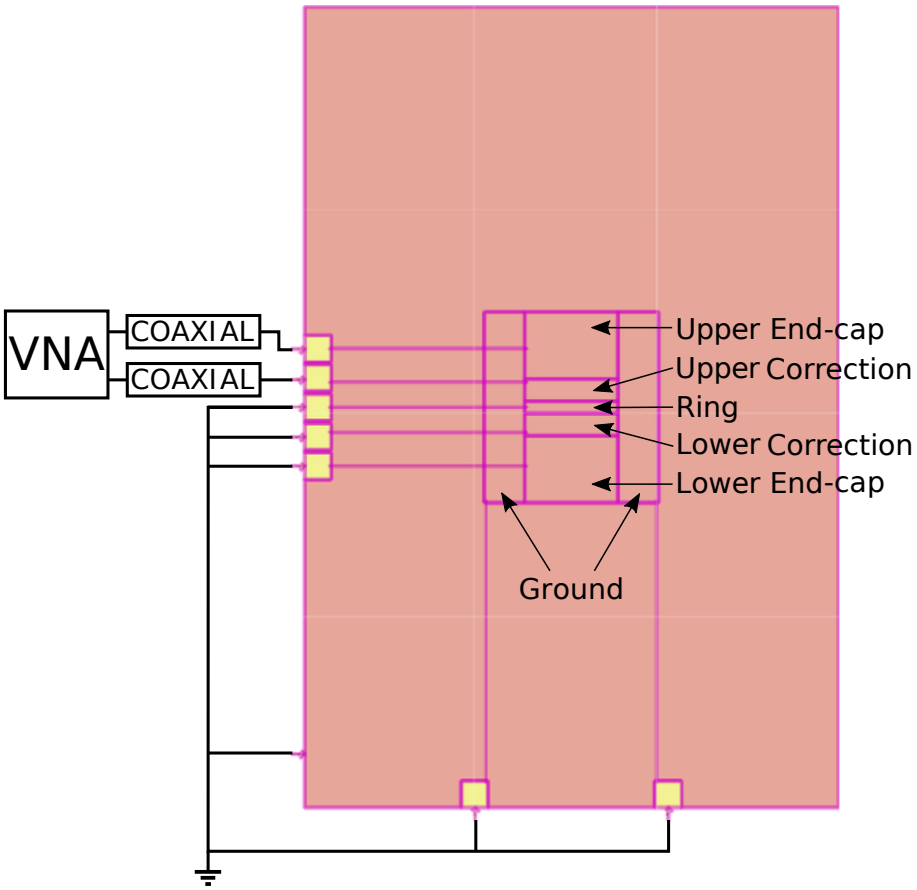


Fig. 4.5 Set up for the measurement of upper End-cap and upper Correction S-parameters with a Π network configuration and grounding the rest of electrodes and Ground Plane. A schematic of the MIR chip has been used for this representation, however the measurement set-up is similar for every chip measured in this chapter.

4.2.3 *T* network set-up for measurements

Equally as in the case of Π Network measurement described above, the electrodes that are not being measured and the Ground Plane are connected to ground, as shown in figure 4.4. However, in this case both ports of the VNA are connected to the same electrode of the chip. This can be observed in figure 4.6, where both ports are connected to the Upper End-cap electrodes while the rest of the chip is grounded. The version of the chip used in the example of set-up of figure 4.6 is the MIR chip, introduced in section 4.3, however the configuration is similar for the other models of chip.

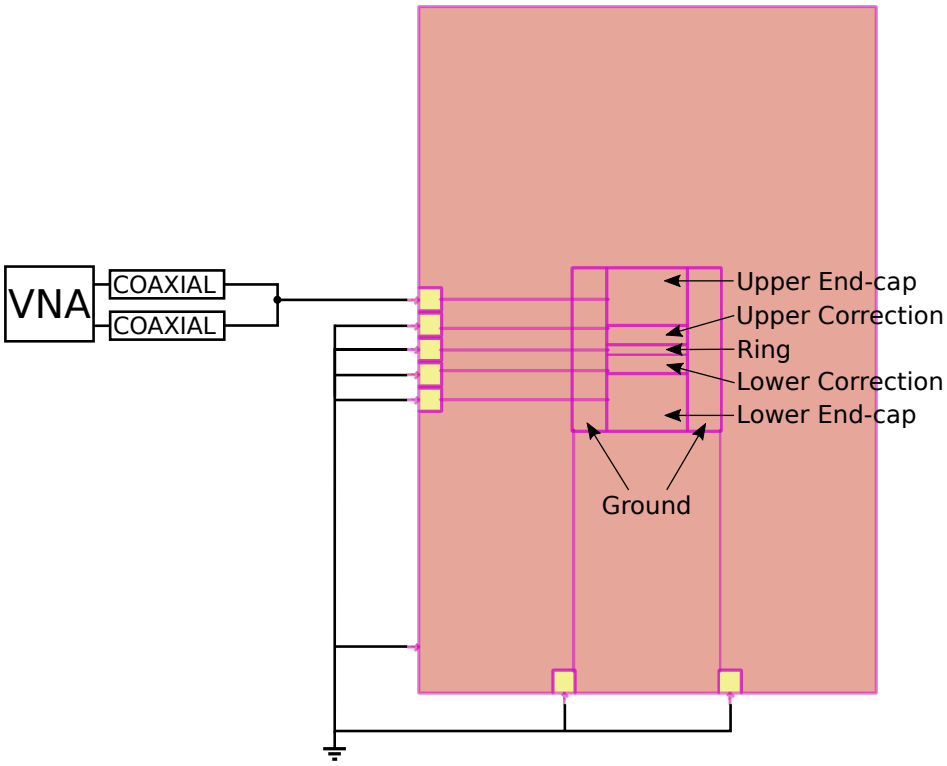


Fig. 4.6 Set up for the measurement of upper End-cap S-parameters with a *T* network configuration and grounding the rest of electrodes and Ground Plane. A schematic of the MIR chip has been used for this representation, however the measurement set-up is similar for every chip measured in this chapter.

4.3 MIR chip

The microfabricated chip was designed by J.Pinder in collaboration with MIR Enterprises [75]. The design of the chip (Figure 4.7) includes seven electrodes: two End-caps, two Corrections, the Ring and two side electrodes (described in section 2.2.4) and seven pads to connect every electrode. The pads are placed on the border of the chip, to facilitate the connection with the rest of the system, and they are connected to the electrodes through buried wires with a width of 3 µm. There is a gap of 10 µm as a separation between different parts of the chip and all is surrounded by a Ground Plane. The dimensions of this chip are shown in figure 4.8.

The top of the chip is covered by a 300 nm layer of alloy composed of gold 80% and silver 20%, used as conductor material. Under this metallization, there is a substrate layer of 900 nm of silicon dioxide and finally a layer of 675 µm of Silicon that holds the structure. The pads are connected to the electrodes through wires buried 400 nm deep into the silicon dioxide layer. The buried wires and the VIAs that connect the top layer with them are

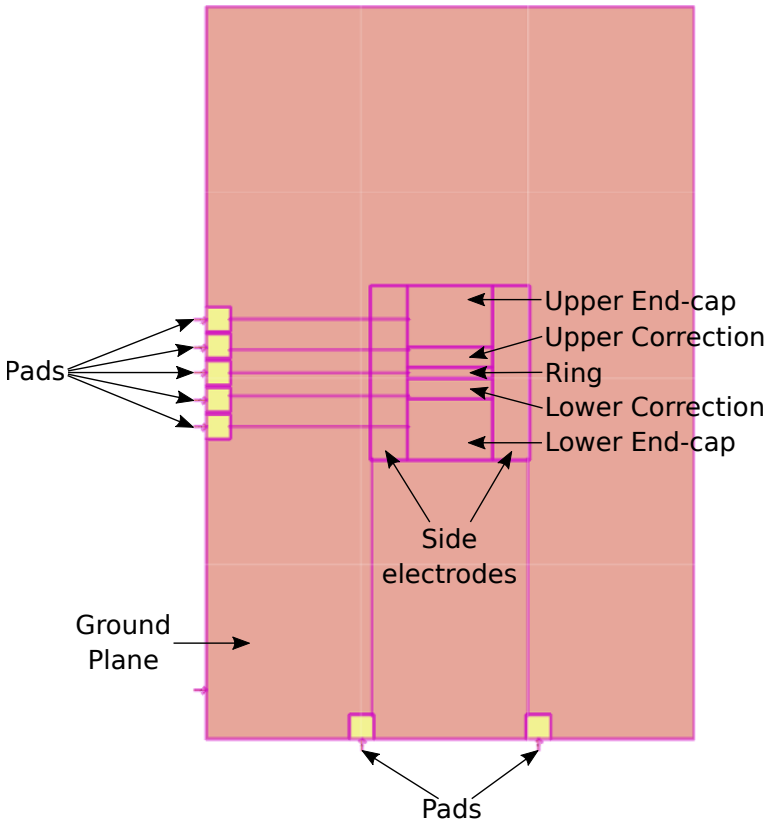


Fig. 4.7 Model of the MIR chip in ADS simulator.

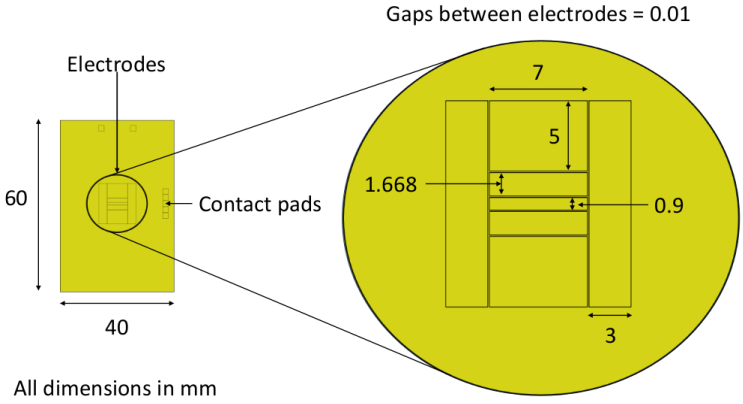


Fig. 4.8 Dimensions of the MIR chip [14].

made of the same gold-silver alloy described before. This structure and dimensions can be easily understood observing the figure 4.9.

4.3.1 Set-up of MIR chip measurements

The VNA is connected to the chip through the PCB board of figure 4.10, which is wire-bonded to the pads of the chip using 25.4 µm diameter aluminium wire, as appears in the photography of the microscope shown in figure 4.11. As it can be observed in figure 4.10,

Fig. 4.9 Substrate of the MIR chip in the ADS simulator. The thickness and material of every layer of the substrate are indicated on the right of the figure. The 'hole' mark represents the via and 'cond' and 'cond2' represent the gold-silver alloy layers.

five SMA connector are soldered to the board to connect the VNA. Both, the chip and the PCB board, are fixed to a PTFE board with nylon screws.

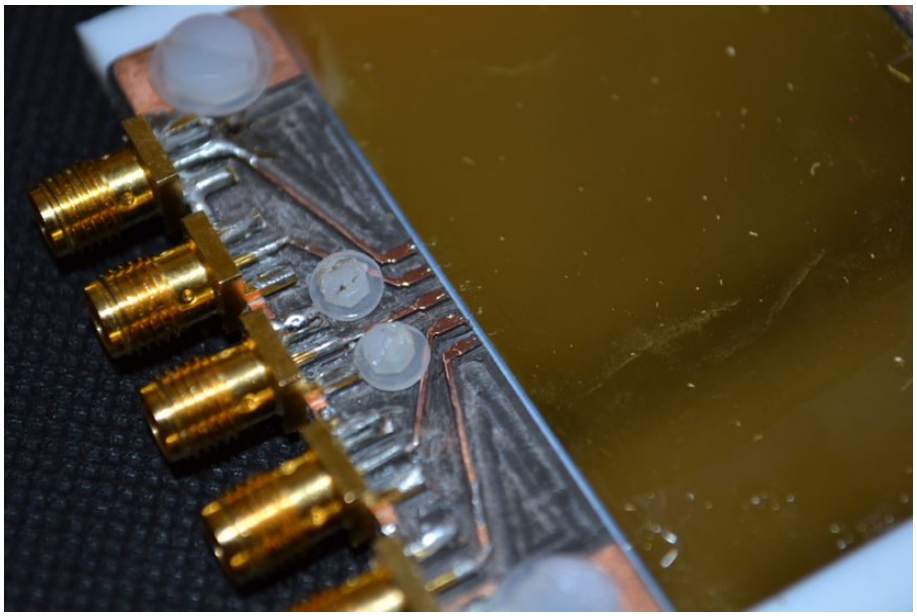


Fig. 4.10 MIR Chip wire-bonded to the PCB board. Both of them are fixed to a PTFE board.

Another SMA connector is soldered over an additional piece of PCB connected to the Ground Plane. Hence, the Ground Plane is doubly grounded through this connector and through the PCB board of figure 4.10.

Finally, every electrode that is not connected to the VNA, is connected to ground. It is done by short-circuiting the SMA with a conductor wire of tin. A picture of this set-up, for a measurement of the chip with Π network configuration through the Ring and upper End-cap ports, is shown in figure 4.12.

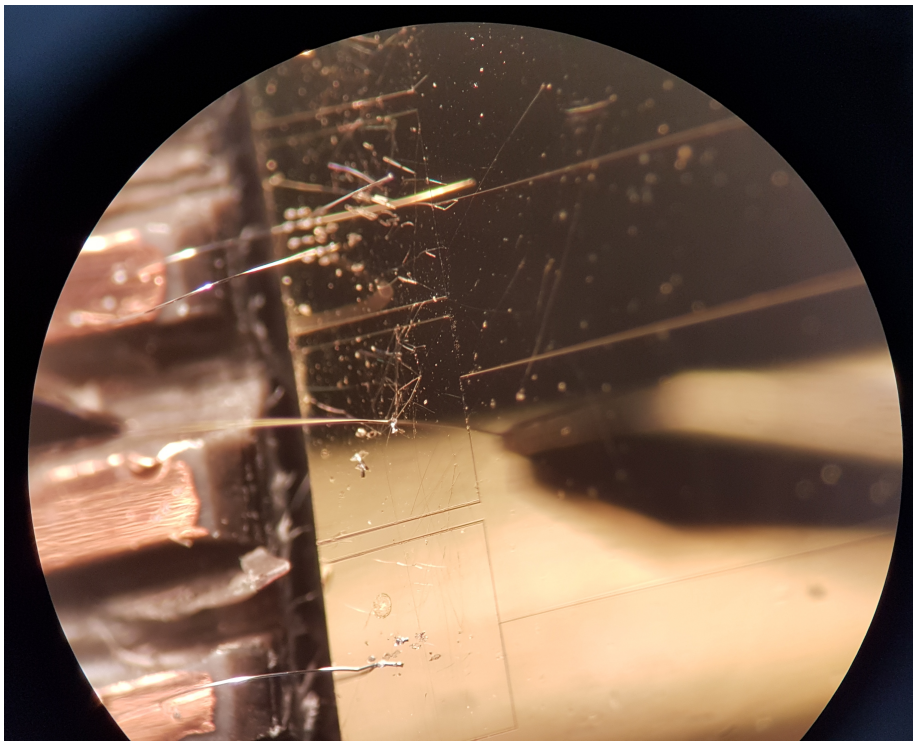


Fig. 4.11 Aluminium wire of 25.4 µm diameter bonding the Pads of MIR Chip to the PCB board. Picture taken using a microscope.

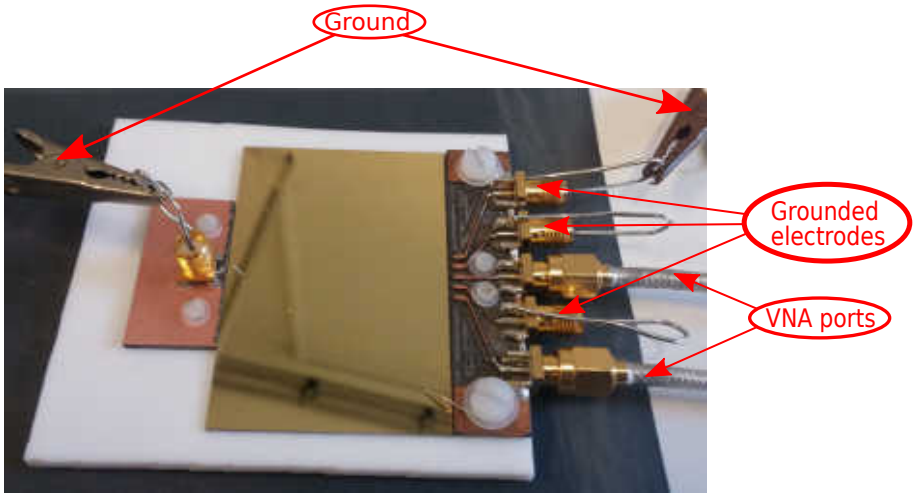


Fig. 4.12 Measurement of the S-parameters of upper End-cap and upper Correction ports of the wire-bonded MIR chip with earth connection on grounded electrodes.

4.3.2 Effects of the PCB board used for wire-bonding

The PCB board used to connect the chip to VNA, as it has been described in section 4.3.1, introduces some parasites that modify the results of measurement of the chip. In this section, this board is measured without the chip attached in order to calculate the effect of the board on the capacitance value.

The board is measured only between the upper Correction and Ring connector, using the Π network model described in section 4.2.2. Two different set-ups are measured: with and without a capacitor of nominal value 4.7 pF connected between the pads of the board, which is a value of capacitance of the same order of magnitude as the capacitances of the chip (the values of the capacitances of the chip are analysed in next sections). A picture of the board with the capacitor connected can be observed in figure 4.13.

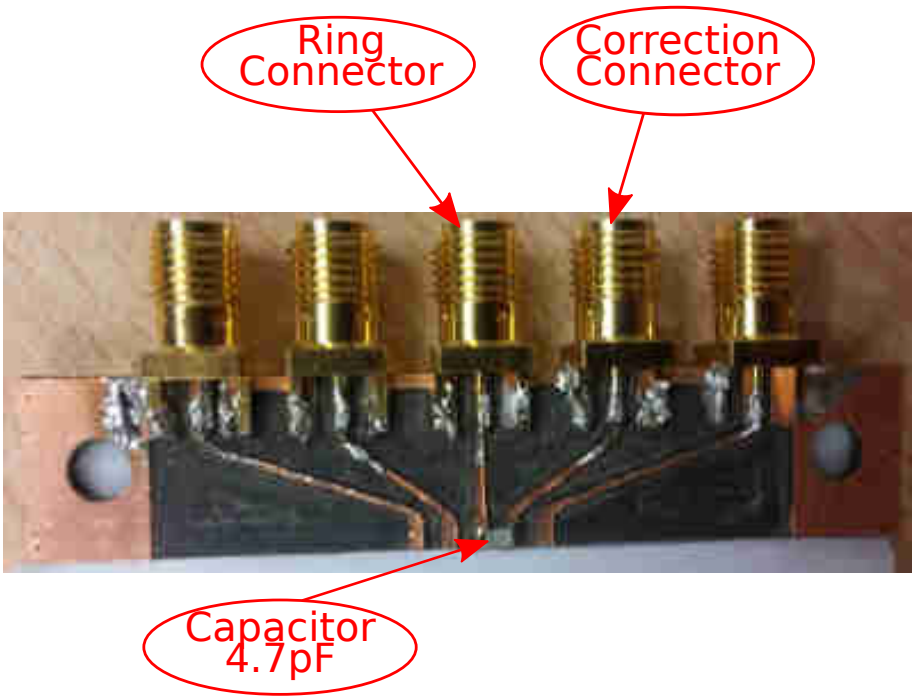


Fig. 4.13 Wire-bonded board with capacitor of 4.7 pF.

The values of $Y_{coupling}$ for both measurements of the board, with and without 4.7 pF capacitor, are shown in table 4.1. These values prove that the effect of the board is very small compared to the value of the capacitance of the chip.

$Y_{coupling}$	Capacitance (pF)	Error (pF)
With 4.7 pF capacitor	4.58	0.02
Without capacitor	8.58×10^{-4}	1.71×10^{-5}

Table 4.1 Capacitances $Y_{coupling}$ between Ring and Correction electrodes connectors of the PCB board with and without capacitor of nominal value 4.7 pF.

4.3.3 Wire-bonded MIR chip

The data presented in this section show the results of the equivalent circuit extract from the measurements of S-parameters of the MIR chip wire-bonded to the PCB board described above. it is measured following the Π configuration introduced in section 4.2.2.

Figure 4.14 is a representation of the coupling admittances between electrodes. The symmetry between the upper and lower End-cap and between the upper and lower Correction electrodes can be observed.

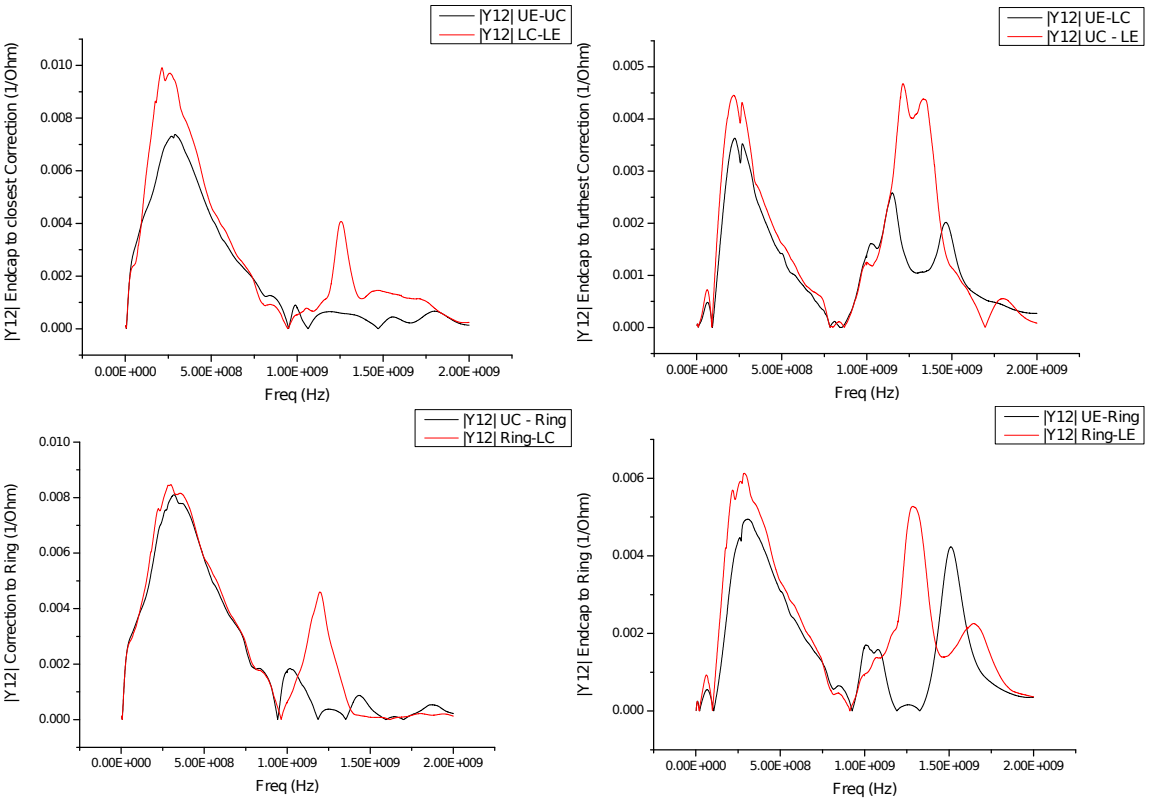


Fig. 4.14 Symmetry between the Upper and Lower electrodes in the wire-bonded MIR chip.

The capacitances shown in tables 4.2 and 4.3 are extracted from a fit of the resonances of figure 4.14. Although there are several resonances represented, the capacitances listed in the tables correspond to the fir of the peaks with bigger capacitances. The analysis shows the calculated values of Y_{in} for the Lower electrodes are significantly higher than the values of the same parameter for the Upper electrodes. This effect is repeatable after several measurements of the chip, which means that there is a physical difference in the chip or in the wire-bonding connection.

Electrodes	Value ± Error		
	C (pF)	$R_s(\Omega)$	L (nH)
Upper End-cap	52.72±0.45	48.76±0.1	25.38±0.08
Upper Correction	55.28±0.31	50.08±0.02	24.83±0.06
Ring	53.16±0.28	54.3±0.1	25.25±0.05
Lower Correction	65.85±0.36	51.1±0.1	29.77±0.06
Lower End-cap	80.02±0.44	53.6±0.1	37.42±0.08

Table 4.2 Weighted mean of capacitances Y_{in} for every electrode of the wire-bonded MIR chip.

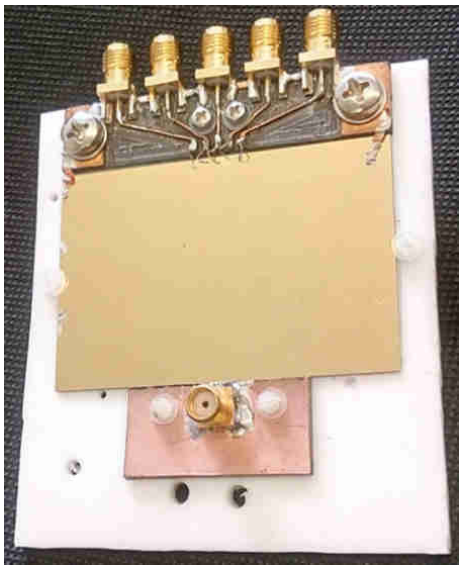
Electrodes	Value ± Error		
	C (pF)	$R_s(\Omega)$	L (nH)
Lower Correction to lower End-cap	10.8±0.08	99.6±0.4	44.4±0.2
Lower End-cap to Ring	4.24±0.03	160±0.8	74.2±0.4
Lower Correction to Ring	7.99±0.08	116.4±0.6	40.0±0.2
Upper Correction to lower Correction	3.69±0.02	161.3±0.7	78.7±0.3
Upper Correction to Ring	6.77±0.06	120.9±0.6	43.9±0.2
Upper End-cap to Ring	3.20±0.07	216±3	75.8±0.1
Upper End-cap to lower End-cap	247±1	2.98±0.02	297±1
Upper Correction to upper End-cap	54.5±0.1	6.52±0.05	108.2±0.5

Table 4.3 Weighted mean of capacitances $Y_{coupling}$ for every electrode of the wire-bonded MIR chip.

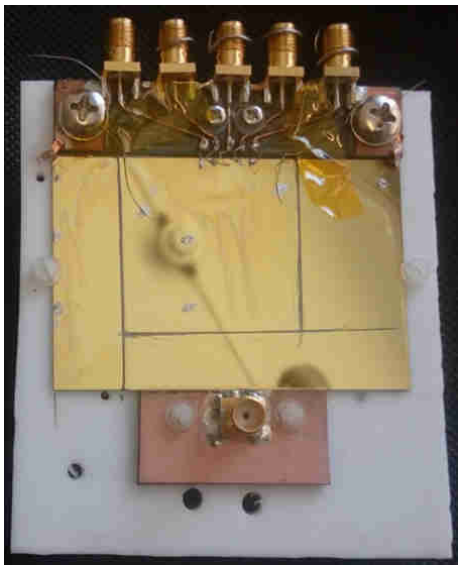
In conclusion, two problems appear. The first one is related to the high input impedance between the electrodes and ground, which deteriorates the quality factor Q as described in section 4.1. The second problem appears due to the high values of losses, which are modelled with the value of the resistance. This last value comes mostly from the buried wires, and it destroys the resonance when the chip is connected to the superconducting resonator, as described in [14]. The next sections show the results of other measurements to confirm the source of capacitance and resistance. The conclusions are finally exposed in section 4.3.6.

4.3.4 Broken and scratched MIR chip

In order to see how the surface of the Ground Plane affects to the capacitance of the chip, the parasitic values of a MIR chip with the Ground Plane scratched and broken are measured. In this case the measurements are done following the T network model described in section 4.2.3. The three set-ups of the chip: scratched, broken and normal, appear in figure 4.15.



a)



b)

c)

Fig. 4.15 Picture of the a) Normal MIR chip; b) Scratched MIR chip; c) Broken MIR chip.

The values of capacitances that have been measured for the three different set-ups are shown in table 4.4 for upper Correction electrode and in table 4.5 for upper Endcap electrode. The capacitance is clearly decreased by scratching and breaking the chip, which means that there is a capacitance created in the interface between the Ground Plane and the silicon layer on the bottom.

Set-up	Capacitance(pF)	Error(pF)
Normal	70.05	0.82
Scratched	58.04	0.10
Broken	54.58	0.23

Table 4.4 Capacitance in the scratched and broken MIR chip measured from Upper Correction electrode.

Set-up	Capacitance(pF)	Error(pF)
Normal	69.83	0.64
Scratched	57.44	0.21
Broken	49.44	0.29

Table 4.5 Capacitance in the scratched and broken MIR chip measured from Upper End-cap electrode.

4.3.5 Wire-bonding buried wires of MIR chip

The main source of losses in the MIR chip is the buried wires, as explained in [14]. Therefore, if this assumption is true, bypassing the buried wires must reduce the resistivity R. The bypassing is done by wire-bonding the pads of the chip to the electrodes. A picture of this appears in figure 4.16.

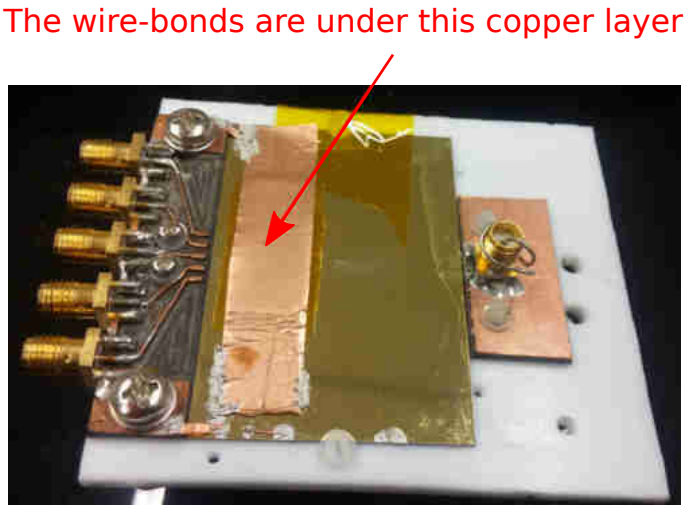


Fig. 4.16 MIR chip with bypassed buried wires by wire-bonding the pads to the electrodes.

To avoid the increment of capacitance between electrodes, a GND copper layer is placed over the wire-bonding (figure 4.17).

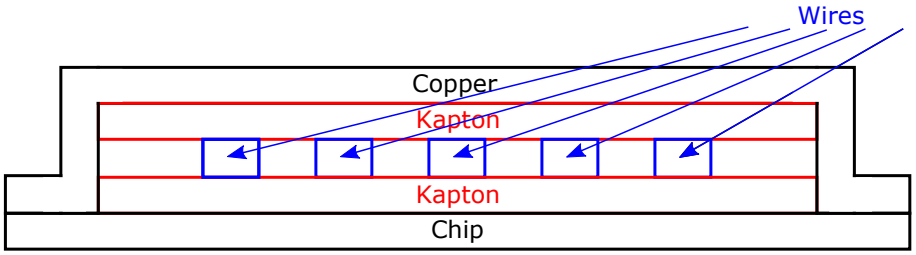


Fig. 4.17 MIR chip with wire-bonded buried wires.

The VNA is connected to the chip as shown in figure 4.18, following a T network model described in section 4.2.3. The final impedance is equal to the sum of the impedances of SMA connector, PCB connection board and wire-bonding.

Also, a flat resonator introduced in chapter 5.1.3 is connected following the schematic of figure 4.18 in order to evaluate the effect on the resonance of a resonator coil. The results of this measurement are fitted using the model of figure 4.19 and presented in table 4.6. The resistivity of the buried wires is reduced as expected, but the capacitance, due to the coupling between the wire-bonding wires, is increased. Therefore, it is a confirmation of the previous assumption about the important contribution of the buried wires to the resistivity of the chip.

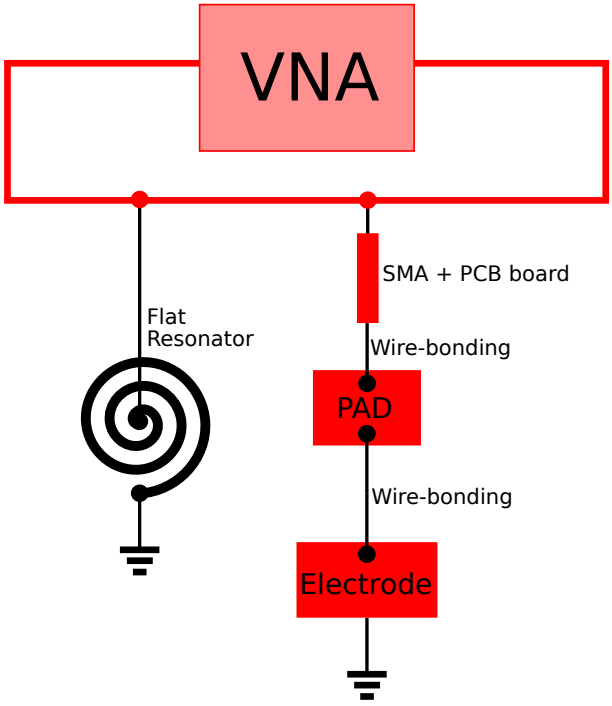


Fig. 4.18 MIR chip with wire-bonded buried wires and flat resonator.

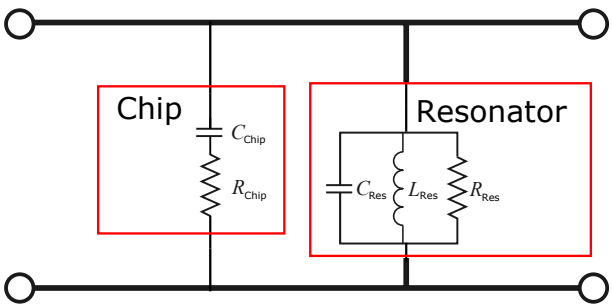


Fig. 4.19 Schematic of the parasitic components of the circuit of figure 4.18.

Set-up	Value ± Error	
	Capacitance (pF)	Resistance (Ω)
Wire-bonded buried wires	356.01±2.53	29.63±0.25
Non Wire-bonded buried wires	117.06±0.56	72.96±0.40

Table 4.6 Weighted mean of capacitances Y_{in} for every electrode of the wire-bonded MIR chip.

4.3.6 Conclusion MIR chip

Considering all the measurements of the previous section it can be concluded that the MIR chip can not be used in our experiment since the resonance of the coil used for the detection of trapped electrons, as described in section 5.1, vanishes when the chip is connected. The main problems of the chip are:

- Too high resistance: as proved with the measurements of section 4.3.5, this effect is produced mainly by the buried wires. Although the resistance was expected to drop by a fifth of the measured value at room temperature [24, 14], according to the measurement of A.Crindland [14], the resistance of these wires is 1.75 kΩ at room temperature and 950 Ω at 77 K. Hence, in order to decrease this resistance, the cross section area of the buried wires must be increased.

- Too high capacitance: two types of capacitance have been analysed: capacitance between electrodes, known as coupling capacitance and the capacitance between each electrodes and GND, known as input or output capacitance (explained in section 4.2). By increasing the length of the gaps (gaps between electrodes and gaps between electrodes and Ground Plane) both types capacitances can be reduced, however, this length must be small enough to avoid charge building up in these gaps.

  The capacitance between the electrodes and GND is also affected by the substrate of the chip, which is p-doped silicon in this case. This substrate acts as a conductor, adding capacitance to the chip. This is the biggest effect and the worst problem presented by the MIR chip. By choosing a substrate with a lower dielectric constant, for example sapphire, the input/output capacitance values could be reduced.

Therefore a new design of the chip, detailed in the next section, was developed to avoid these problems.

4.4 P.W.Circuits chip

The previous section gives a complete explanation of the problems detected in the microfabricated chip that made the detection of electrons impossible. In order to avoid these problems, the microfabricated chip was replaced by a PCB chip. It was designed by J.Pinder and fabricated by P.W.Circuits Ltd. Additionally, appendix D presents the characterization of a first prototype of this PCB chip made in the our laboratory by J.Pinder before manufacturing the final design.

The results presented in this section are the most important of the high frequency measurements, since the P.W.Circuit chip is currently being used to trap in the Geonium Chip experiment. Many test were done until the techniques described below were developed, providing a method that give stable, repeatable and consistent values for the measurements. As detailed below, the most relevant of these tests are described in this section whilst some other are included in appendixes C and D.

This new model of the chip has no side electrodes, but only five of them: two End-caps, two Correction and the Ring. The electrodes are surrounded by a Ground Plane connected to five circular pads through wires of 0.5mm width, placed over the bottom of the chip. The pads are not surrounded by Ground Plane as in the microfabricated chip, but they are isolated on a rectangular extension of the PCB. The details described here and the dimensions of every part of the chip can be observed in figure 4.20.

The top of the chip is covered by a copper layer of 0.03 mm and over a 0.5 mm layer of alumina (Al_2O_3) as a substrate. On the bottom of the chip there is another 0.03 mm layer of copper for the wires, that connect to pads and electrodes through copper VIAs. The pads are circular with a hole in the centre to facilitate the connection with a screw to other elements of the experiment. A picture of one of these chips can be observed in figure 4.21.

Finally, in order to reinforce the chip and improve its resistance, a 0.168 mm layer of substrate RO4350B is manually attached to the bottom of the chip. This improvement becomes specially important during the sealing process of chip and inner cryogenic chamber described in section 3.1.7, as it prevents the chip from cracking or being physically damaged. Although it is used on the chip during the trapping process, the chip used in the measurements of this chapter has no reinforcement, since the effects of this layer are considered to be negligible in the high frequency measurements.

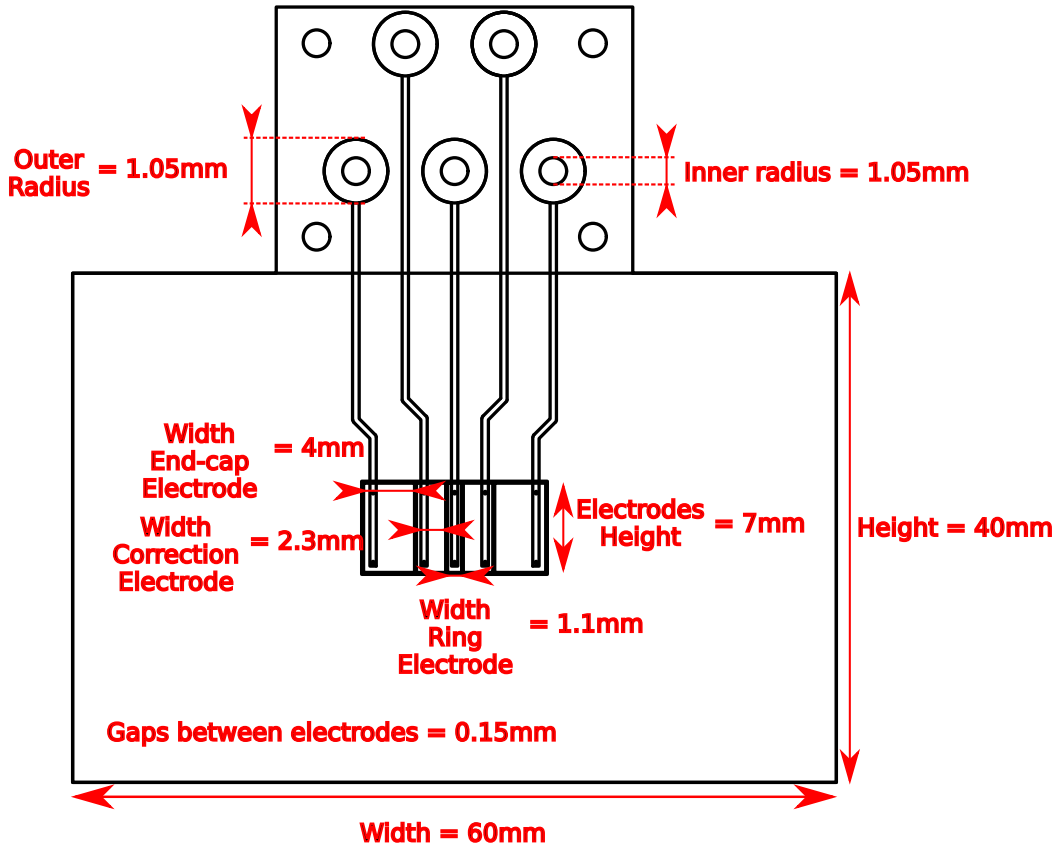


Fig. 4.20 CAD and dimensions of the P.W.Circuits chip.

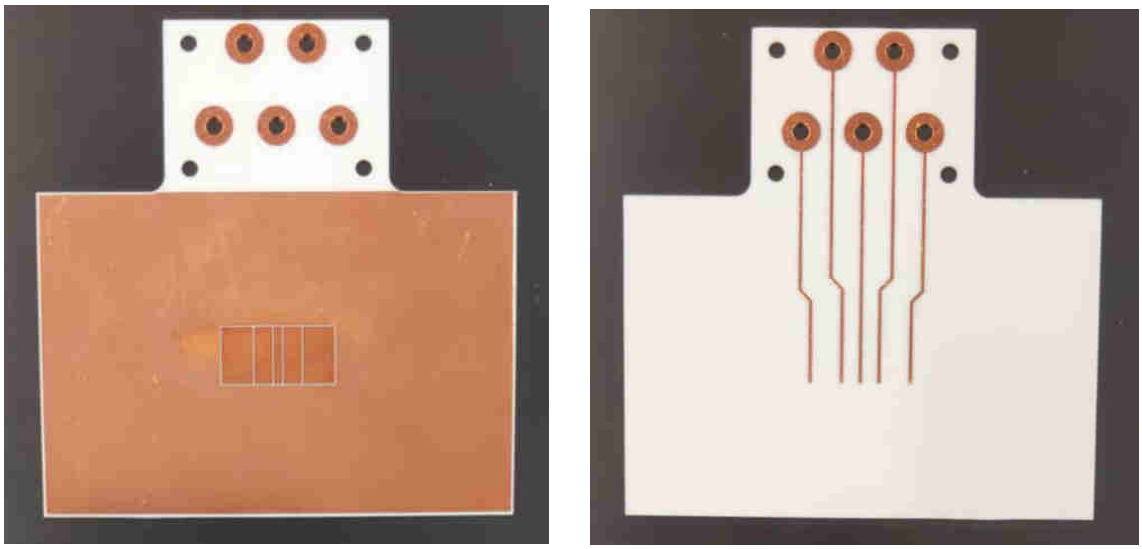


Fig. 4.21 a) Top and b) Bottom of the P.W.Circuits chip.

4.4.1 Set-up of P.W.Circuit chip measurements

The set-up presented in this section is the one that provided the most accurate and consistent results. However, several alternatives were tested until this optimum solution

was developed. The appendix C details one of these previous tests, done with SMA connectors crimped to terminals that were attached to the chip with nylon screws. This method was dismissed as the measurements were not consistent enough, measuring variations in the results every time, due to the change of position of the connectors in the different repetitions and to the high precision of the VNA used to measure it. The set-up introduced below solves this problem by soldering the SMA connectors to the chip.

As can be observed in figure 4.20, the P.W.Circuit Chip has a group of pads separated from the rest of the chip, facilitating external connections. Since the high frequency measurements could be modified by variations in the connection set-up, some SMA connectors need to be affixed to these pads in order to get a measurement as consistent and realistic as possible.

Firstly, the connection to ground, short-circuited to the Ground Plane of the chip, is necessary to solder the ground of the SMA connectors. The copper from the pads is removed using a scalpel and a copper tape layer is placed over this region. Five holes are cut on the copper layer to make possible the connection between the pin of the SMA connectors and the pads on the bottom of the chip. This is shown in figure 4.22.

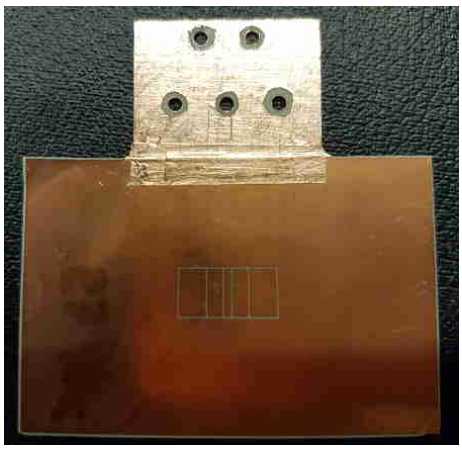


Fig. 4.22 P.W.Circuit Chip with pads removed and a copper tape layer covering the pads part of the chip.

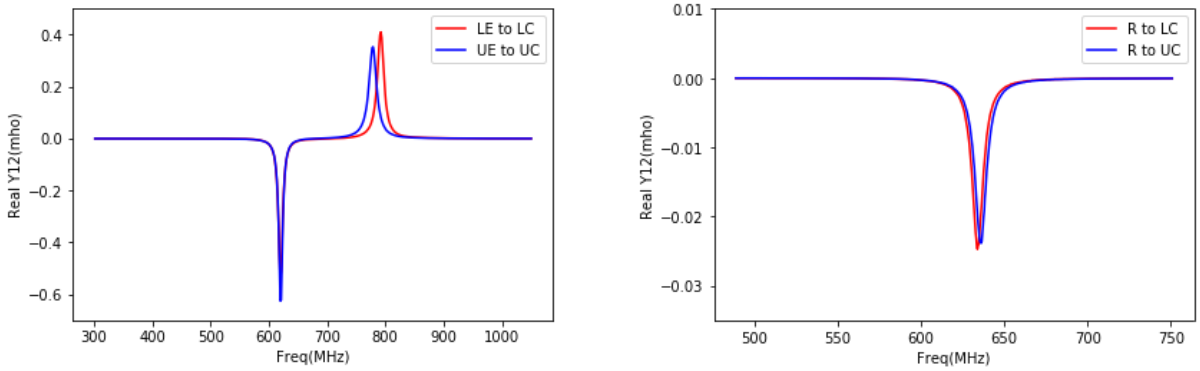
Secondly, five SMA connectors are attached, one to every pad of the chip. The pin of the SMA connectors is introduced through the VIA and soldered to the pad on the bottom (figure 4.23.b), while the outer part is soldered to the copper tape on the top (figure 4.23.a).

a) b)

Fig. 4.23 a) Top and b)bottom of the P.W.Circuit Chip with SMA connectors soldered to the pads.

4.4.2 P.W.Circuit chip high frequency measurements

The P.W.Circuit chip is measured with a Pi method as described in section 4.2.2. The Y-parameters obtained with the measurement of the coupling between electrodes are shown in figure 4.24, where the symmetry between electrodes can be observed. By fitting these data as described in section 4.2, the values of the capacitance, resistance and inductance of tables 4.7 and 4.8 are calculated. Although several resonances appear in every graph, the values of the tables are shown only for the peaks with bigger capacitances in every case.



a) b)

Fig. 4.24 Symmetry of the real part of the coupling impedances between a)End-caps and Correction electrodes and b)Ring and Correction electrodes.

Electrodes	Value ± Error		
	C (pF)	$R_s(\Omega)$	L (nH)
Lower End-cap	1.22±0.003	2.32±0.005	54.34±0.10
Lower Correction	3.52±0.002	0.82±0.0004	18.70±0.009
Ring	1.12±0.006	2.71±0.02	58.68±0.33
Upper Correction	3.14±0.002	0.88±0.0006	20.91±0.01
Upper End-cap	1.21±0.005	2.21±0.01	54.30±0.23

Table 4.7 Results of the fitting for the coupling between every electrode of the P.W.Circuit chip and GND.

Electrodes	Value ± Error		
	C (pF)	$R_s(\Omega)$	L (nH)
Lower End-cap to lower Correction	1.92±0.0008	1.5±0.0008	34.35±0.01
Lower Correction to Ring	1.60±0.001	1.94±0.002	40.73±0.03
Upper Correction to Ring	1.64±0.001	1.97±0.002	39.49±0.03
Upper End-cap to upper Correction	2.06±0.002	1.33±0.001	31.92±0.02

Table 4.8 Results of the fitting for the coupling between electrodes of the P.W.Circuit chip.

4.4.3 Effect of the VIAs, buried wires and SMA connectors

In order to determine the contribution to the total coupling capacitance of the chip produced by the buried wires and SMA connectors to the total coupling capacitance of the chip to the pads, two measurements are done. Firstly, the chip is measured without electrodes, secondly, the board of the chip is cut measuring only the SMA connectors soldered to the pads.

For the first case the electrodes of the chip are removed with a scalpel. a picture of the chip with no electrodes is shown in figure 4.25. The results of coupling capacitances between different pads of the chip, extracted from the the VNA measurements, are listed in table 4.9. The values of the capacitances are smaller than the ones measured with the chip with electrodes. Hence, it can be concluded that the main contribution to the coupling capacitance of the chip is the effect of the coupling capacitance between electrodes.

In the second case, only the SMA connectors soldered to the pads are measured. As shown in figure 4.26, the part where the pads are soldered to the electrodes is cut from the rest of the chip. The measures of these connectors give no clear resonances, proving that this is a negligible contribution to the total capacitance of the chip.

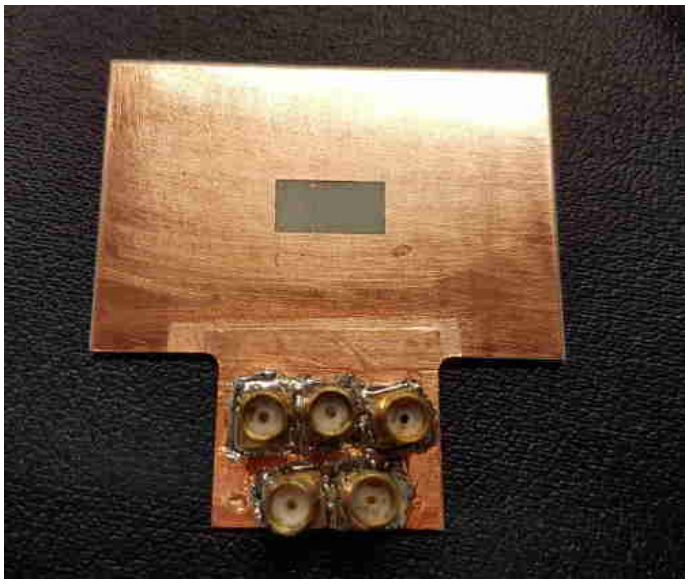


Fig. 4.25 P.W.Circuit Chip without electrodes.

Electrodes	Capacitance (fF)	Error (fF)
Lower End-cap to lower Correction	80.92	0.46
Lower Correction to Ring	95.18	0.37
Ring to Upper Correction	13.40	0.02
Upper Correction to upper End-cap	14.30	0.03

Table 4.9 Weighted mean of the coupling capacitances between the pads that connect every electrode of the P.W.Circuit Chip without electrodes.

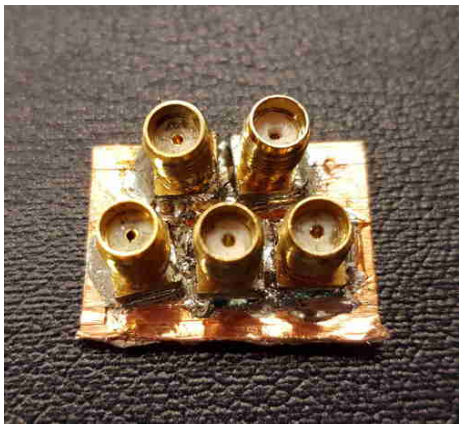


Fig. 4.26 SMA connectors soldered to the pads. The rest of the chip has been removed to measure only the capacitance of this part.

4.4.4 P.W.Circuit with flat resonator

This measurement is the most relevant among the high frequency measurements of the chip, since it provides a clear and empirical evidence that a resonator of similar

characteristics to the one used in the Geonium Chip experiment can be observed whilst it connected to the P.W.Circuit chip.

The measurement of the input capacitance of every electrode, that means, the capacitance between the electrode and GND, proves that they are considerably smaller than the values of the MIR chip. In order to check that these values are small enough to detect a resonator when the chip is connected, the flat resonator of section 5.1.3 is connected following the schematic of figure 4.27. The system is measured using the T model described in section 4.2.3.

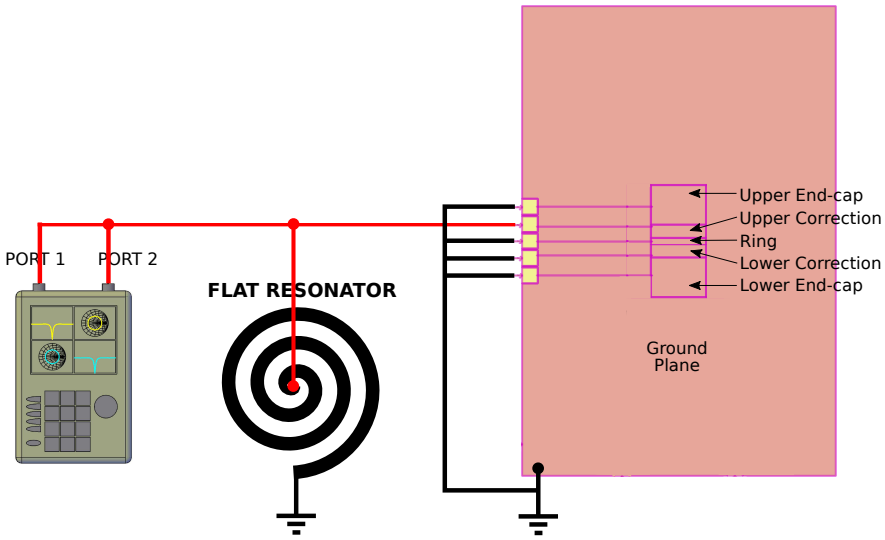


Fig. 4.27 PWCircuit chip connected to the flat resonator.

A comparison of the results of this system and the data of the resonator measurement without attached chip are listed in table 4.10, showing that the highest contributor to the total capacitance is the resonator itself, while the contribution of the chip is smaller than 10%. Additionally, figure 4.28 represents the shift of the resonant frequency, showing that the resonances are visible with a chip connected to the resonator through the Correction electrode.

These results are conclusive and prove that the effect of connecting the P.W.Circuits chip is small enough to detect the resonator, meaning that the values of the parasitic components of the chip in this case are acceptable for the requirements of the experiment.

Electrode connected to the resonator	Capacitance (pF)	Error(pF)
Only resonator without chip	84.42	0.08
Lower End-cap	90.24	0.76
Lower Correction	91.11	0.07
Ring	89.96	0.65
Upper Correction	90.64	0.63
Upper End-cap	90.15	0.08

Table 4.10 Weighted mean of the input capacitances of the system composed of the flat resonator with and without the P.W.Circuit Chip, measured from every electrode of the chip.

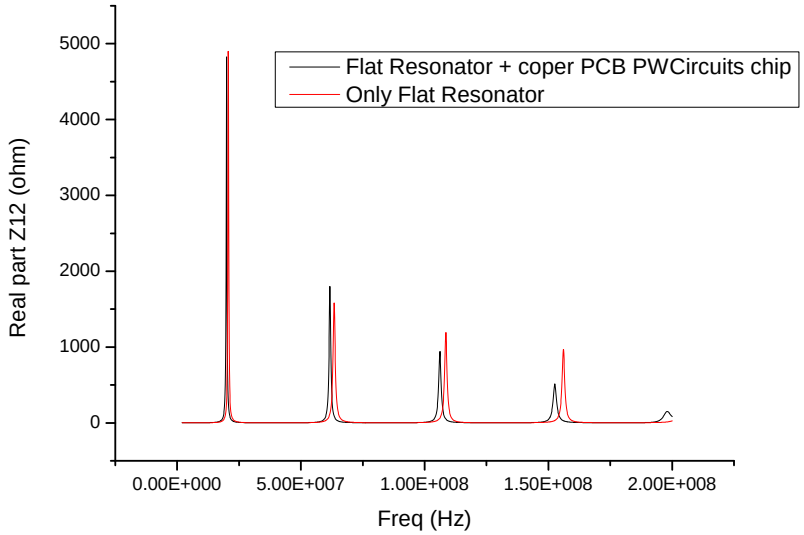


Fig. 4.28 Measurement of the PWCircuit chip connected to the flat resonator through the pad of the upper Correction electrode.

4.5 Conclusion

The input capacitance of the electrodes in the case of the MIR chip was increased by the p-doped silicon substrate, which also has a high dielectric constant. Replacing this with alumina, a material with a lower dielectric constant, in the P.W.Circtuit chip, the capacitance is considerably reduced.

In addition, the gap between electrodes is enlarged in the design of the P.W.Circuit chip, reducing the coupling capacitance.

In conclusion, the values of the parasitic components of the P.W.Circuit chip are acceptable and the trapped electrons could be detected with it.

Chapter 5

Detection system of the trapped electrons

The technical details of the experimental implementation of the detection system are described in this chapter. The theoretical overview is provided in section 2.4, whilst this chapter includes only technical aspects of the fabrication and measurements in order to prove that our experimental system follows the requirements previously described.

The chapter is divided into three sections dedicated to the description of the current resonator used in the experiment and new models of resonator that are currently being developed, the amplifiers and their connection to the chip and the description of a new system that is being investigated and could replace the resonator in future versions. The position of the resonator and amplifiers in the experiment and the connection of the output to the spectrum analyser is shown in figure 5.1.

5.1 Resonator and new designs

As it is described in sections 2.4, 2.5 and 2.6, the resonator is an essential part of the detection system. The resonator currently used in the experiment, which is introduced below, is a cylindrical helical resonator designed by J.Pinder. Although it is working perfectly, it is very big and therefore it occupies an important part of the cryostat.

In this section, some new designs of resonator, with smaller size and working at different frequencies, are analysed. These new models are not being used currently in the

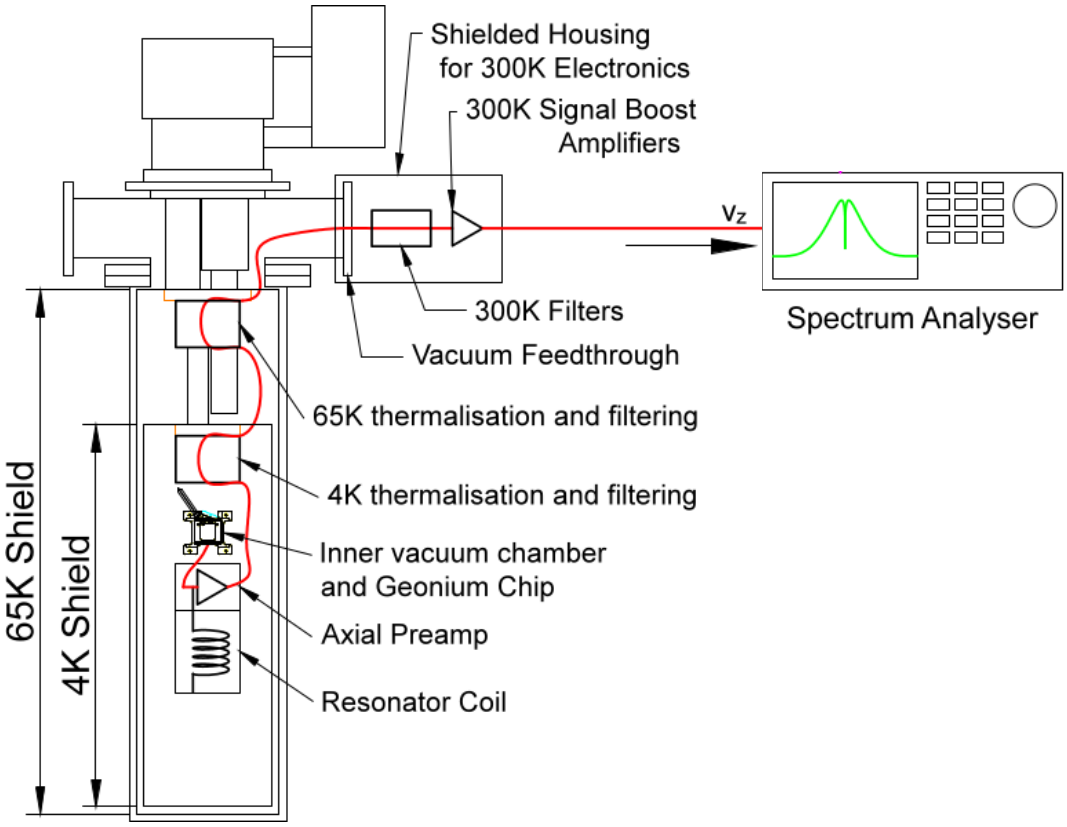


Fig. 5.1 Detection system in the Geonium chip experiment and connection to the external spectrum analyser [75].

experiment, but it is an important improvement for future versions of the Geonium Chip trap.

5.1.1 Cylindrical helical resonator

The cylindrical helical resonator described was designed by J. Pinder [75], following the rules of commonly used resonators for radio frequency communication [30].

The resonator material is pure niobium, which is superconductor below the critical temperature of 9.3 K [75, 81]. The distance to the magnetic source was considered and it was checked that the magnetic field would not introduce any losses and that the Q factor of the resonator would not be reduced. The design and manufacturing procedure of the resonator has been described in more detail in the doctoral thesis of J.Pinder [75].

The size of the resonator is shown in figure 5.3, indicating the values of the resonator dimensions. And a picture of the resonator and its superconducting shield can be observed in figure 5.2.

Fig. 5.2 Picture of the niobium cylindrical helical resonator and shield [75].

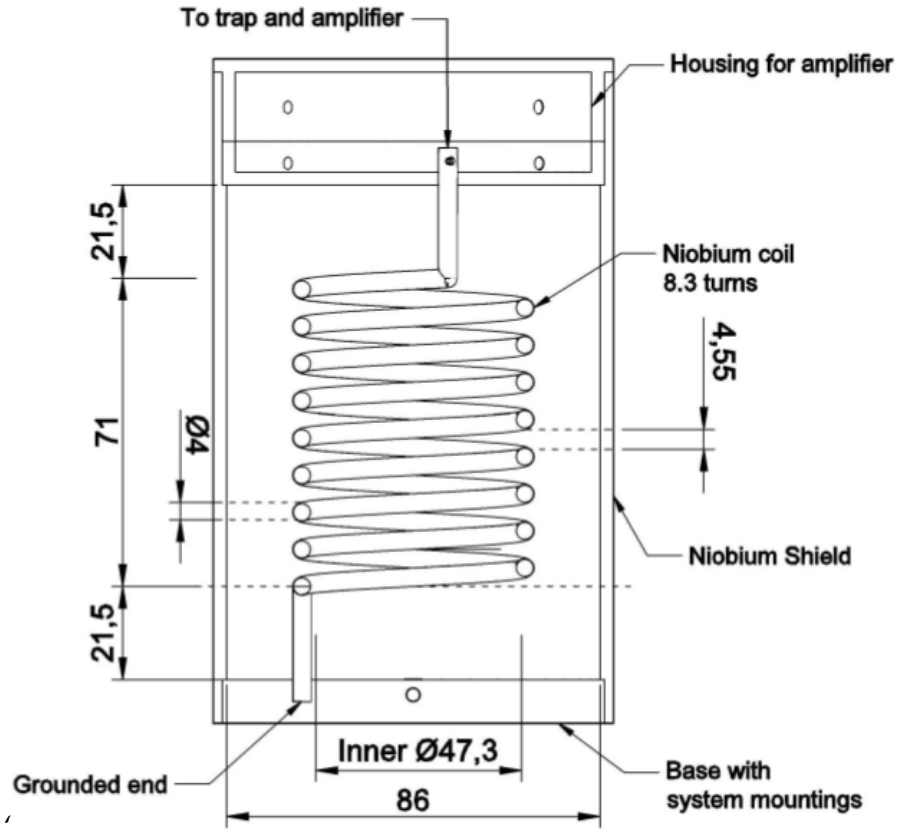


Fig. 5.3 Picture of the niobium cylindrical helical resonator [75].

The resonator has been polished in order to increase the quality factor. The electrical response in frequency of the resonator can be seen in Figure 5.4, which is a comparison of the cylindrical helical resonator Q factor, analysing the cases of the polished and unpolished resonator at different temperatures.

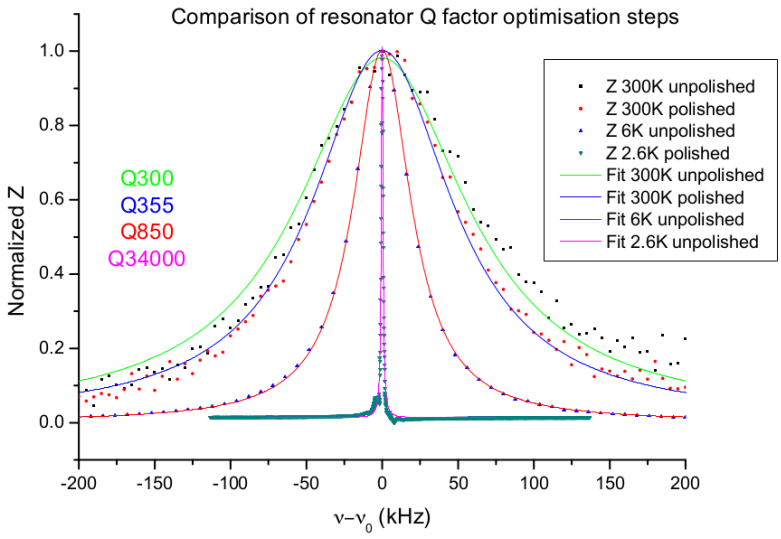


Fig. 5.4 Resonance and Q factor of the unloaded cylindrical helical resonator at different temperatures. The resonator has been measured being polished and unpolished [75].

5.1.2 Superconducting meander resonator

The first design proposed to replace the cylindrical helical resonator is the meander superconducting resonator described in this section.

Design of the meander resonator

A 1 GHz resonator is designed using ADS software. It consists of a superconducting meander-shaped line, with two gaps at both ends of the line, being all this enclosed in a metallic case. The final design is shown in figure 5.5.

Although 1 GHz is too high for the axial frequency of the trapped electrons, it could be within the range of frequencies of the modified cyclotron frequency ω_+ if the magnetic field is small. The modified cyclotron frequency of a trapped electron has not been measured directly yet and it is a challenge that could be achieved in our experiment. Additionally, the resonant frequency depends on the length of the resonator path and it could easily be modified.

High Frequency analysis of the meander resonator

The high frequency properties of this resonator are measured with the Vector Network Analyser (VNA), connecting each port of the VNA to each port of the resonator, indicated in figure 5.5. The S parameters of the system are obtained and transformed to Z parameters in order to calculate the values of the equivalent circuit components, as explained below.

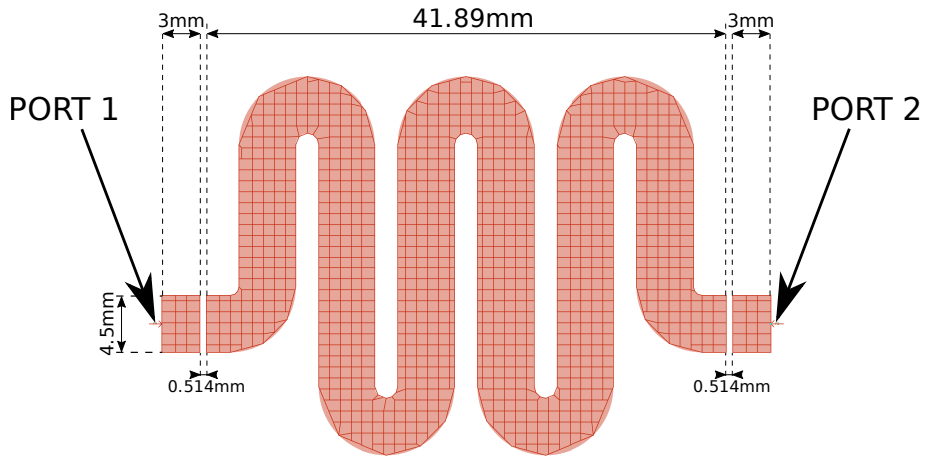


Fig. 5.5 Design of the superconducting meander resonator in ADS.

A complete introduction to the high frequency analysis, S and Z parameters, can be found in appendix B.

According to the description of the equivalent circuit for Z parameters given in appendix B.2.4, it could be described as a T network, as depicted in figure 5.6.

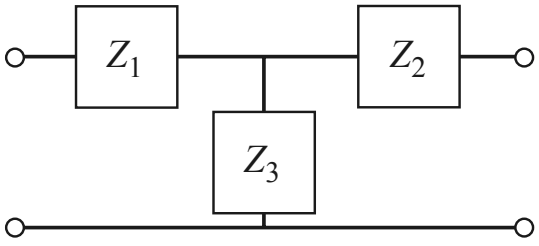


Fig. 5.6 Z parameter model of the resonator [77].

And the impedance matrix in the T network is

$$\begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} = \begin{pmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{pmatrix}, \tag{5.1}$$

where it is obvious that $Z_1 = Z_{11} - Z_{12}$, $Z_2 = Z_{22} - Z_{12}$ and $Z_3 = Z_{12}$.

Following the system of figure 5.6, the design of figure 5.5 is modelled as the equivalent circuit that appears in figure 5.7, where the resonant frequency is determined by the length of the line and the parameters C_1, R_1, C_2 and R_2 by the width of the gaps, following a similar procedure to the one described in [38].

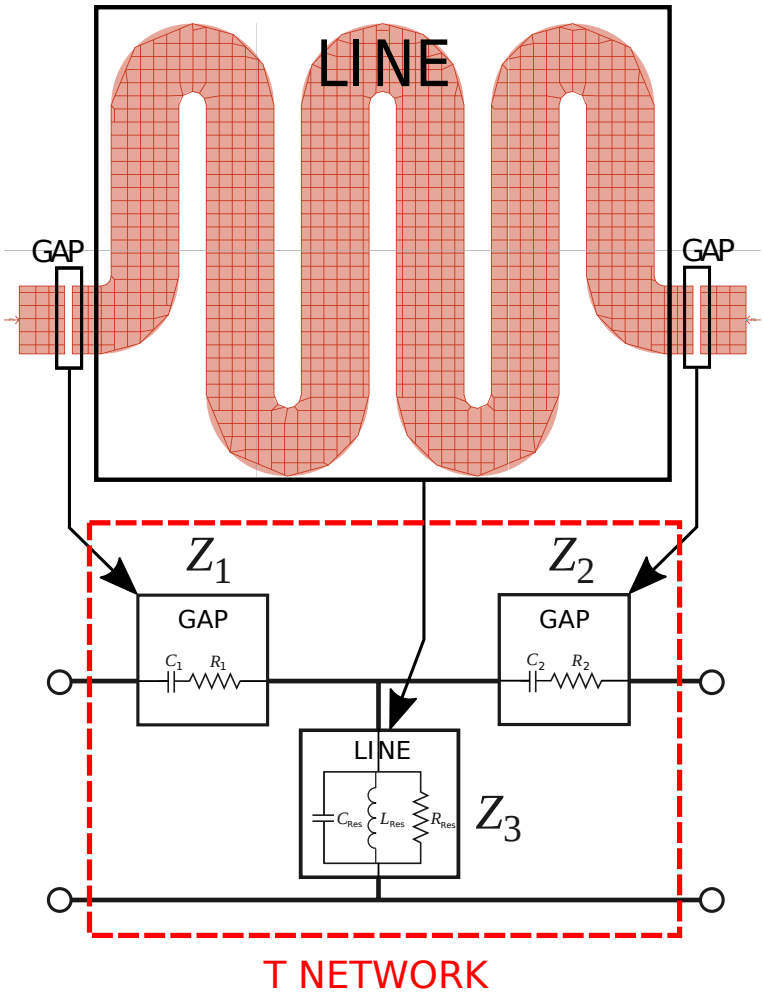


Fig. 5.7 Equivalent circuit to the designed resonator.

In this case Z_1, Z_2 and Z_3 are [38]

$$Z_1 = Z_{11} - Z_{12} = R_1 + \frac{1}{i\omega C_1}, \tag{5.2a}$$

$$Z_2 = Z_{22} - Z_{12} = R_2 + \frac{1}{i\omega C_2}, \tag{5.2b}$$

$$Z_3 = Z_{12} = \left(i\omega C_{res} + \frac{1}{i\omega L_{res}} + \frac{1}{R_{res}} \right)^{-1}. \tag{5.2c}$$

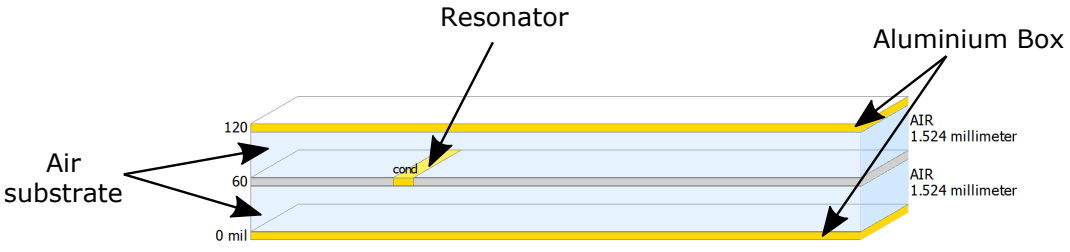


Fig. 5.8 The resonator substrate is simulated as air, since it is held by very small and thin PTFE sticks.

Simulation of the meander resonator

The resonant frequencies are easily identified in figure 5.9, where the parameter Z_{12} is represented. These resonances appear, approximately, at frequencies equal to n · 1 GHz, with $n = 1,2,3\ldots$

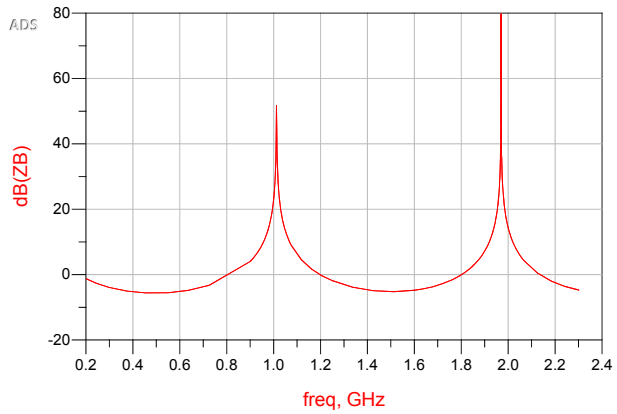


Fig. 5.9 Z_{12} for the meander resonator in the ADS simulation.

Using the value of the Z parameters obtained in the simulation at resonant frequency 990 MHz and equations 5.2c, the results are

$$R_1 = 9.72\ \Omega \tag{5.3a}$$

$$C_1 = -8.10\ pF \tag{5.3b}$$

$$R_2 = 9.73\ \Omega \tag{5.3c}$$

$$C_2 = -8.10\ pF \tag{5.3d}$$

$$R_{res} = -4.85\ \Omega \tag{5.3e}$$

$$C_{res} = 25.85\ pF \tag{5.3f}$$

$$L_{res} = 1\ nH \tag{5.3g}$$

The simulated quality factor for the resonance at 1 GHz is

$$Q = \frac{\omega_0}{\Delta\omega} = 11404.51 \tag{5.4}$$

where ω_0 is the central frequency and $\Delta\omega$ is the bandwidth of the peak.

Manufacturing of the meander resonator

The circuit is manufactured using a *High-Z CNC table* machine in our laboratory. The chosen material for the cavity is aluminium, whilst NbTi is used for the resonator (figure 5.10).

The material of the meander part is Nbti, which is superconductor below 9.3 K [75, 81]. It is chosen in order to minimize the resistance of the resonator. These losses of the material could be modelled as a resistor in series with the resonator and its effect decreases the height of the resonant peak. Hence, minimizing the resistance of the resonator by using superconducting material improves the Q factor.

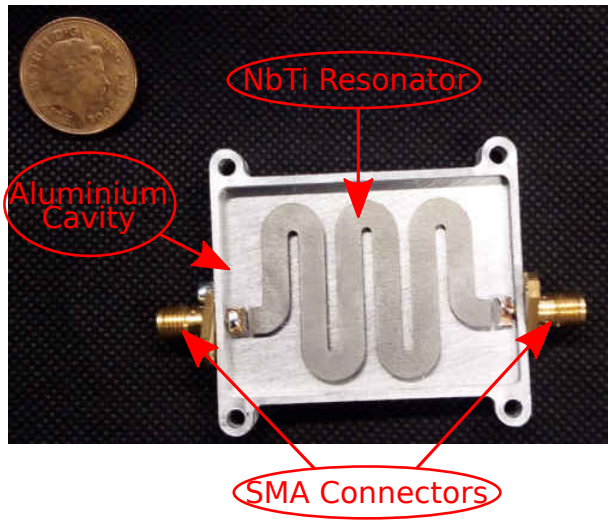


Fig. 5.10 The NbTi resonator in the aluminium cavity.

Room temperature measurements of the meander resonator

The resonator is measured, as described above, with a VNA connecting both ports. This measurement is done at room temperature and the results are shown in figure 5.11.

If equations 5.2c are applied to the measurement of Z_{12} at resonant frequency 983.8 MHz, the value of the electronic components of the equivalent circuit are

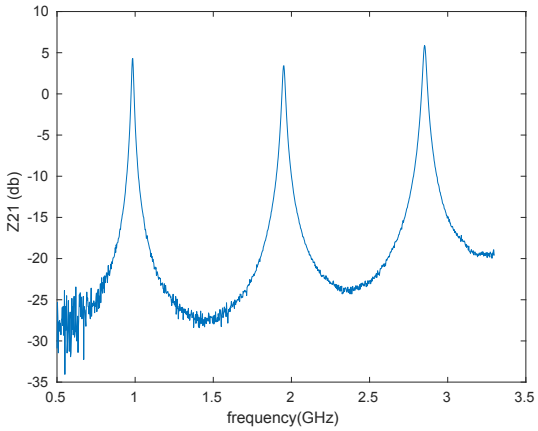


Fig. 5.11 Z_{12} measured with VNA.

$$R_1 = 0.31\ \Omega \tag{5.5a}$$

$$C_1 = 2.92\ pF \tag{5.5b}$$

$$R_2 = 1.38\ \Omega \tag{5.5c}$$

$$C_2 = 2.89\ pF \tag{5.5d}$$

$$R_{res} = 1.67\ \Omega \tag{5.5e}$$

$$C_{res} = 26.17\ pF \tag{5.5f}$$

$$L_{res} = 1\ nH \tag{5.5g}$$

The quality factor for the manufactured resonator at the same frequency is

$$Q = \frac{\omega_0}{\Delta\omega} = 68.39 \tag{5.6}$$

ω_0 being the central frequency and $\Delta\omega$ the bandwidth of the peak.

As it could be observed in figure 5.11, similar to the simulation, there are some harmonics at frequencies n $\cdot$ 1 GHz, n=1,2,3... The calculation of the Q factor at these frequencies (table 5.1) shows that the Q factor of the different peaks increases with the frequency, since the width of the peaks does not change significantly for the peaks at higher frequencies, obtaining a higher value with the equation 5.6.

Frequency	Q factor
983.8 MHz	68.39
1.95 GHz	94.13
2.85 GHz	118.70

Table 5.1 Q factor at resonant frequencies.

5.1.3 Flat spiral resonator

In this section, the design of a flat resonator formed by a spiral is discussed. Replacing the cylindrical helical resonator with this one would considerably reduce the occupied space in the cryogenic chamber.

Design of the flat spiral resonator

The flat spiral resonator is designed and simulated using ADS software. The chosen substrate for this first prototype is *Duroid 5880*, a commonly used substrate made of the dielectric material PTFE and copper as conductor, and with the dimensions of figure 5.12.

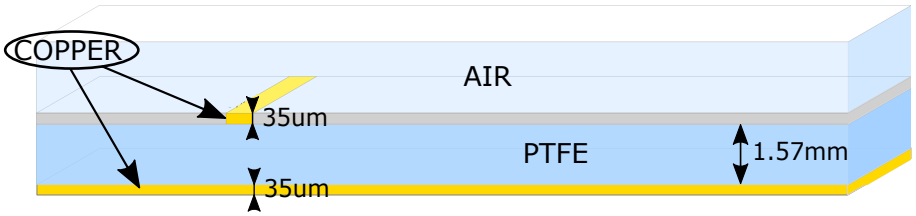


Fig. 5.12 Substrate Duroid 5880 in ADS.

The final model of the resonator in ADS software is shown in figure 5.13.

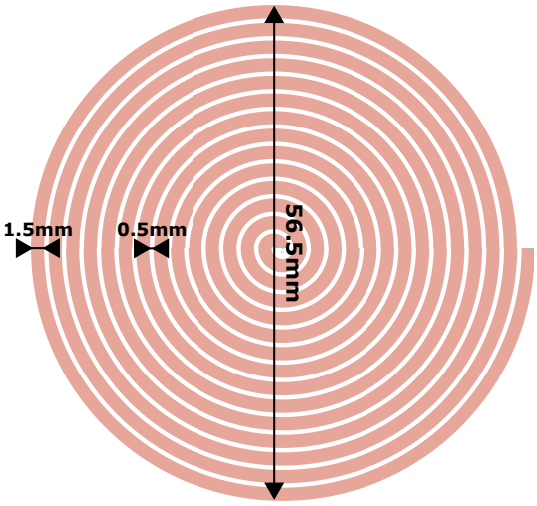
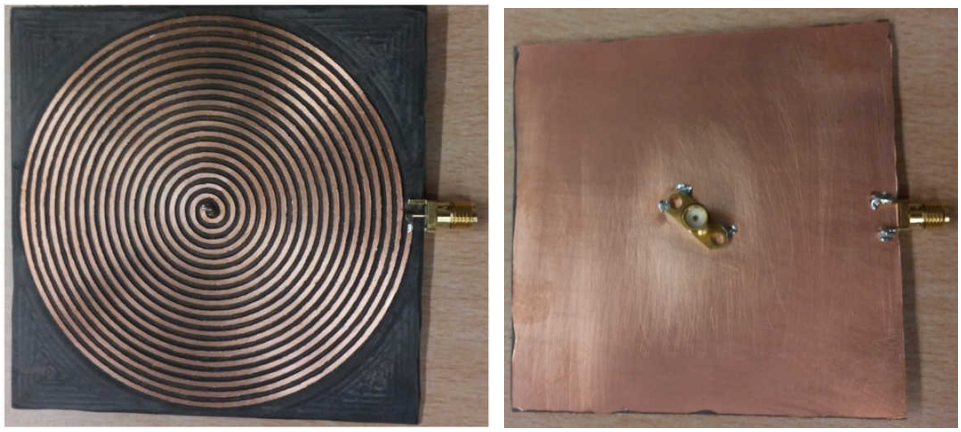


Fig. 5.13 Design of the resonator in ADS software.



(a) (b)

Fig. 5.14 Flat Resonator. Picture of the a)top and b)bottom.

This model of figure 5.13 is manufactured in our laboratory with a *High-Z CNC table* machine and two SMA connectors soldered to the end of the spiral. The final resonator is the one of figure 5.14.

High frequency analysis of the flat spiral resonator

The flat resonator is measured with the VNA, obtaining the S parameters and converting it into Z parameters, in order to calculate the value of the high frequency components of the system. An introduction to the high frequency theory, S and Z parameters can be found in appendix B .

The real part of the spiral resonator impedance is fitted using the real part of the impedance obtained from the real inductor model shown in figure 5.15.

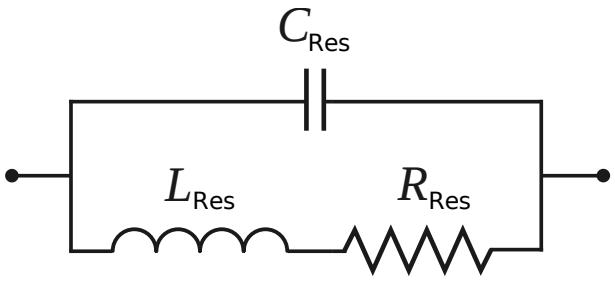


Fig. 5.15 Real inductor equivalent circuit [6], fitted with the values of Z12 in the case of the flat spiral resonator measurement of figure 5.16.

Both ports of the VNA are connected to the central SMA connector shown in figure 5.14, and the connector at the other end of the line is grounded. A schematic of this set-up appears in figure 5.16.

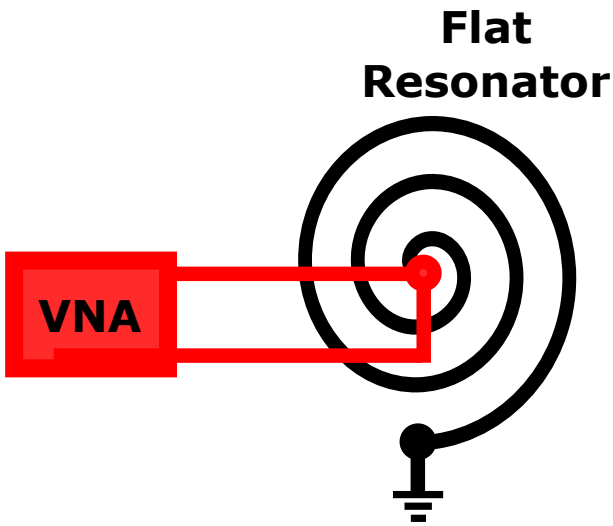


Fig. 5.16 Measurement set-up of the flat resonator in ADS.

According to the theory of Z parameters equivalent circuit given in appendix B.2.4, the system could be modelled as the T network of figure 5.17, where Z_{11}-Z_{12}=0 and Z_{12} is the impedance of the resonator. Therefore, the parameter Z_{12} is the one analysed to see the resonances.

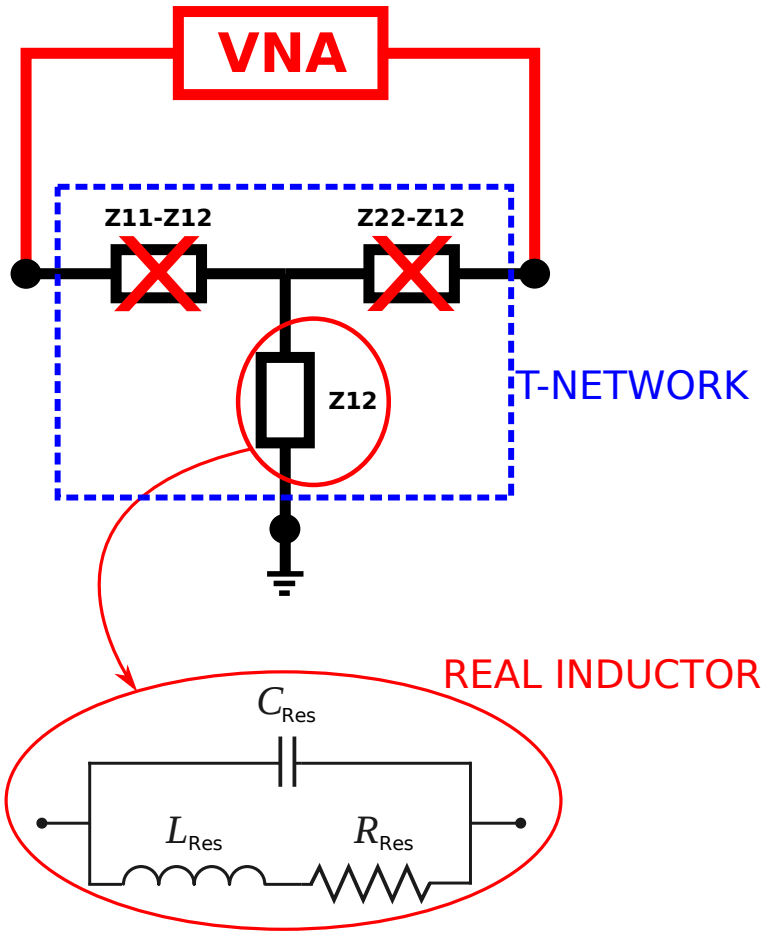


Fig. 5.17 Z parameters model used in the spiral flat resonator measurement.

Simulation of the flat spiral resonator

A resonance appears at 23.00 MHz, and the second and third harmonic at 72.00 MHz and 120.00 MHz respectively, as shown in the Z_{12} representation of the simulation results of figure 5.18.

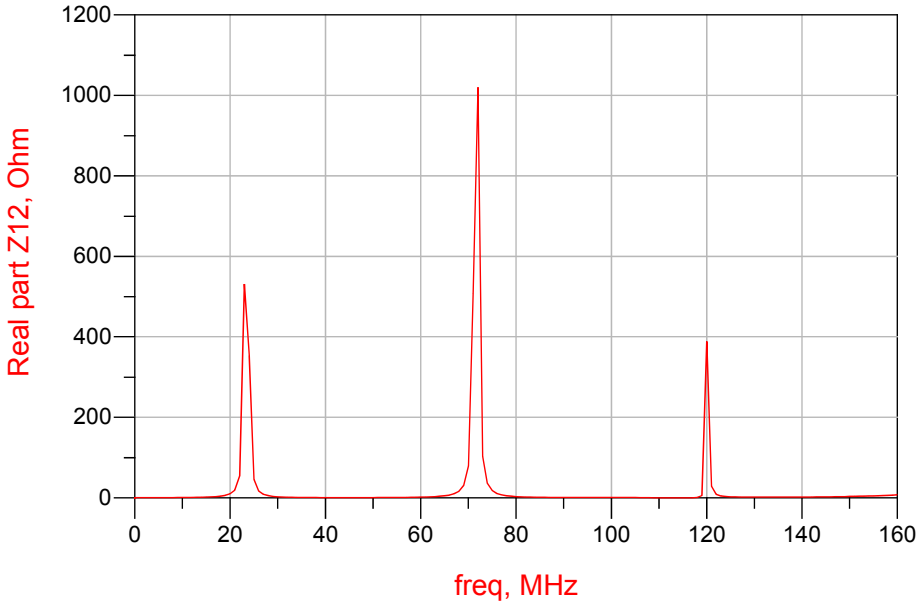


Fig. 5.18 Simulation of the flat resonator in ADS.

The resonant frequency has been experimentally proven to be easily shifted by modifying the length of the spiral, while the thickness of the paths has been chosen to set the characteristic impedance to 50 Ω.

Measurement of the flat spiral resonator

The results of the fabricated resonator measurements are almost identical to the simulated ones. Some variations of the resonator length due to manufacturing errors could explain the small variation in the frequency of the resonances. However, it could be easily readjusted by following more precise manufacturing techniques.

The material used is copper, which includes some losses, which reduces the height of the peaks. Hence, for future versions, the Q factor of this prototype can be improved by using a superconducting material, thus minimising the parasitic resistance of the resonator.

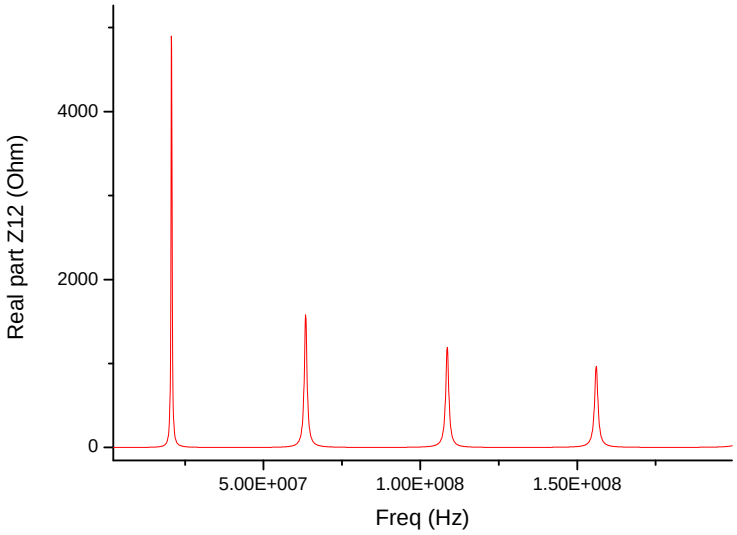


Fig. 5.19 Real part of the Z_{12} parameter from the measurement of the flat resonator with the VNA.

The fit of the first resonant peak of figure 5.19 with the model of a real inductor described in figure 5.15, gives the following values

$$R_{Res} = 0.97 \pm 0.004\ \Omega, \tag{5.7a}$$

$$C_{Res} = 83.20 \pm 0.13\ pF, \tag{5.7b}$$

$$L_{Res} = 0.65 \pm 0.001 \mu\ H. \tag{5.7c}$$

And the measurement of the Q factor

$$Q = \frac{\omega_0}{\Delta\omega} = 90.04 \tag{5.8}$$

The losses are modelled as a resistor in series with the resonator that reduces the Q factor. In order to improve it, the losses in the resonator must be reduced, for example, by replacing the copper that has been used as a conductor by a superconductor material.

5.2 Amplifiers

There are two amplifiers in the system, as can be seen in figure 5.1. The first one at 4 K, known as "Axial amplifier", isolates the trapped electrons removing any noise that

could reach the trap through the cable that connects the rest of the detection system. And the second one, at room temperature, amplifies the signal in order to be detected in the spectrum analyser.

The amplifier at 300 K is a Mini-Circuits ZFL-500LN+ with 24 dB of gain [68]. Although it is sold covered by a metallic box, in the experiment it is placed in an aluminium box fabricated by J.Pinder in the laboratory, in order to give an extra shielding for noise that could penetrate through the connections or the first case of the amplifier.

The Axial amplifier of figure 5.20 and 5.21 was designed by A.Crindland using the model described in [91], since both of them operate at similar frequencies [14]. This amplifier has two GaAs transistors, a *NE25139* dual gate MESFET, manufactured by NEC, at the first stage and an *ATF35143* pHEMT, from Avago technologies, at the second stage. The first one provides the gain and a high input impedance while also reduces the input capacitance (the importance of reducing it is described in section 4.1). The second stage is used to match the output impedance of the amplifier to the 50 Ω of the coaxial line that will connect the amplifier to the rest of the system as described in figure 5.1.

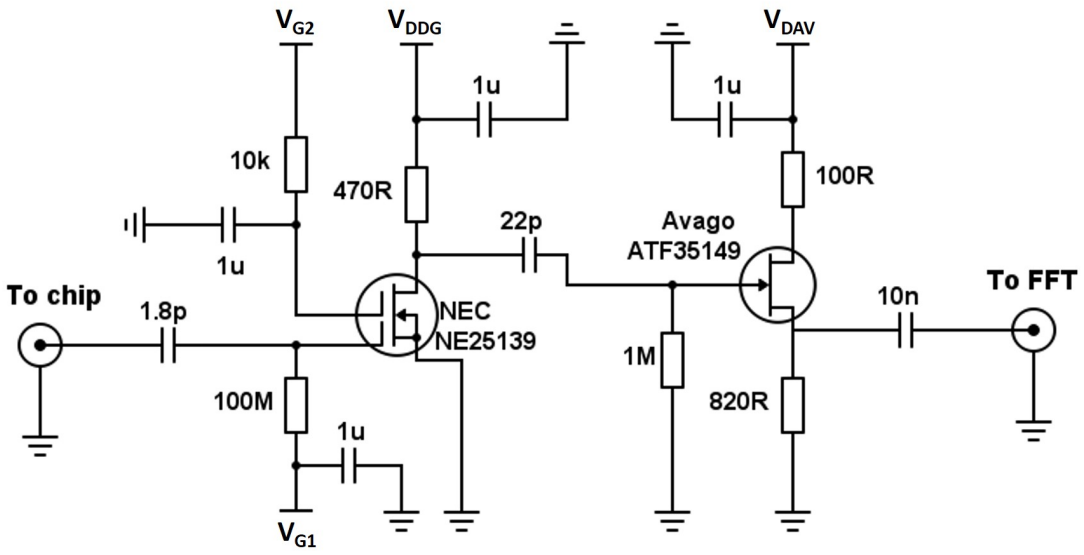


Fig. 5.20 Schematic of the axial amplifier used in the experiment [14].

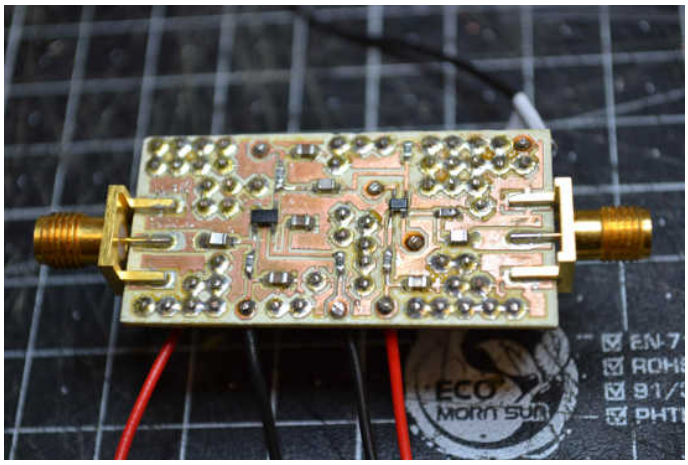


Fig. 5.21 Photo of the axial amplifier used in the experiment [14].

5.3 Replacing the resonator with a resistor

In current Penning Traps experiments, the detection of the trapped particles always requires a resonator, which is one of the biggest devices of the system. Removing it could be another achievement in the reduction of size that the Geonium Chip introduces.

Moreover, the resonators have a narrow resonant peak, which is fixed and restricts the detection only to frequencies close to the resonant frequency. Therefore, the detection of different frequencies would not be possible with the same resonator or it needs to be adapted in order to have a tunable resonant frequency [45], presenting a clear limitation of Penning traps in uses where broad band frequency detection is necessary, such as mass spectrometry.

This section presents a novel solution consisting of replacing the big resonator with a small SMD resistor, that works as a universal compact detection system of the trapped particles. Due to the important implications of these results, this is one of the main sections of this thesis.

The resistor is placed over the pads connected to the Correction electrodes of the chip - Although it is also possible to use the Ring, only the connection between both Correction electrodes has been investigated in these first experiments. The first part includes a theoretical explanation of the proposal and in the last part some measurements are included to prove that it is viable. Although the idea has been proven to be possible, the research on this topic is still being developed and more progress needs to be done before it can be installed in the experiment.

These experiments focus on the axial frequency of the electron in the Geonium Chip, which is typically between 30 MHz and 90 MHz [1]. It implies that other frequencies of heavier particles can be measured too, for example, the cyclotron frequency of a proton which, in the example of [1], is 15 MHz for B = 1 T.

In accordance with the explanation above, this section develops a broadband universal detection system. However, it could present limitations since the dip created by the particles over the impedance frequency spectrum of the resonator has to be visible. The width of the dip, as described in section 2.6, depends on the ratio q^2/m, where q and m are the charge and mass of the trapped particle respectively, according to equations 2.47 and 2.51. For very low values of this ratio, that means, for particles with a very big mass comparing to the charge, the dip is very narrow and undetectable. Therefore, the detection system is universal, considering particles with a reasonable q^2/m ratio, such is the case of a single electron and a single proton, as shown in this section.

5.3.1 The idea of replacing the resonator

As introduced in section 2.4.1, in the current detection systems the trapped ion induces a current between the correction electrode and GND that generates a voltage across the resonator. Since the resonator is replaced by a resistor conected to both Correction electrodes, as shown in figure 5.22, the current would circulate through the resistor, thus generating a voltage between both Correction electrodes. This is amplified by a differential amplifier before it can be detected by the spectrum analyser.

Considering ${q'}_{ind}$ as the charge induced by the trapped ion over one of the Correction electrodes and ${q''}_{ind}$ the charge induced over the other Correction electrode,

$$ {q'}_{ind}\left(\mathbf{r}\left(t\right)\right) = -q\frac{1}{4\pi}\int\int_{\Sigma} dx'dz' \left.\frac{\partial G(\mathbf{r}\left(t\right)|x',y',z')}{\partial y'}\right|_{y'=0}, \tag{5.9} $$

$$ {q''}_{ind}\left(\mathbf{r}\left(t\right)\right) = -q\frac{1}{4\pi}\int\int_{\Sigma} dx''dz'' \left.\frac{\partial G(\mathbf{r}\left(t\right)|x'',y'',z'')}{\partial y''}\right|_{y''=0}, \tag{5.10} $$

the current induced on these electrodes is

$$ I_{ind}\left(t\right) = \boldsymbol{\nabla}\Delta q_{ind}\left(\mathbf{r}\right)\cdot\dot{\mathbf{r}}\left(t\right) \tag{5.11} $$

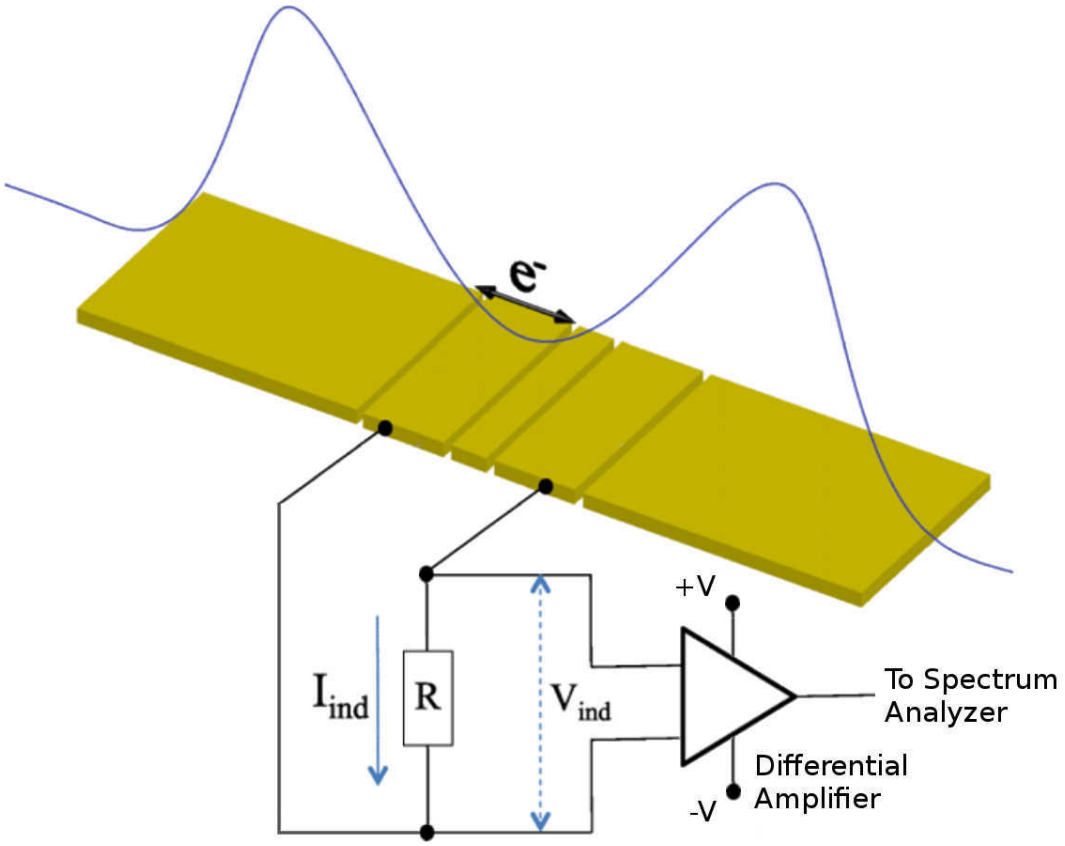


Fig. 5.22 New detection system with a resistor between the Correction electrodes and connection to a external spectrum analyser.

where $\Delta q_{ind} = q''_{ind} - q'_{ind}$.

5.3.2 Equivalent circuit to the resistor with the trapped ion

As seen in section 2.6, the equivalent circuit of the trapped electron can be modelled as an inductor L_{ion} in series with a capacitor C_{ion}. Moreover, the effect produced by fluctuations of the trapped ion frequency is modelled as a resistance R_{ion}. This resistor has no physical meaning but it is only a mathematical tool.

On the other hand, the chip with the attached resistor is modelled with the equivalent circuit of a real resistor described in [6], where the sum of the capacitive, inductive and resistive effects of the resistor and the chip are represented by the parameters $C_{parasitic}$, $L_{parasitic}$ and R respectively.

The final circuit is shown in figure 5.23.

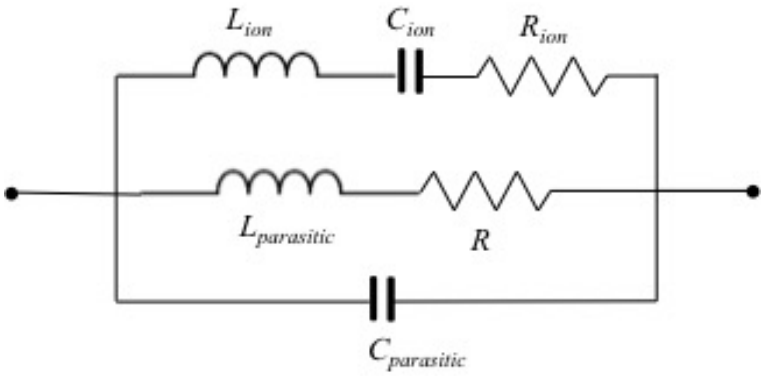


Fig. 5.23 Equivalent circuit to the electron trapped by a chip with a resistor between the Correction electrodes.

5.3.3 Effect of the resistor in the capacitance

In order to evaluate the effect of the resistor over the total capacitance of the chip, the capacitance of the resistor alone and the chip with the attached resistor are compared. If the capacitance added by the resistor is too high, the detection of the trapped electron would not be possible.

The different systems are measured using a VNA, obtaining the S parameters and converting it to admittance parameters to estimate the parasitic components of the resistor.

Firstly, an SMD resistor of 24.8 kΩ of the company *Stackpole Electronics Inc.* is soldered to two SMA connectors, as shown in figure 5.26. It is measured with the VNA, connecting each port of this device to each pad of the resistor. According the Π model described in appendix B.2.4, the parasitic capacitance of the resistor is extracted by fitting the impedance of the coupling of both ports $1/-Y_{12}$ with the model of a real resistor of figure 5.24 [6]. A representation of the Π model set-up used for this measurement is shown in figure 5.25.

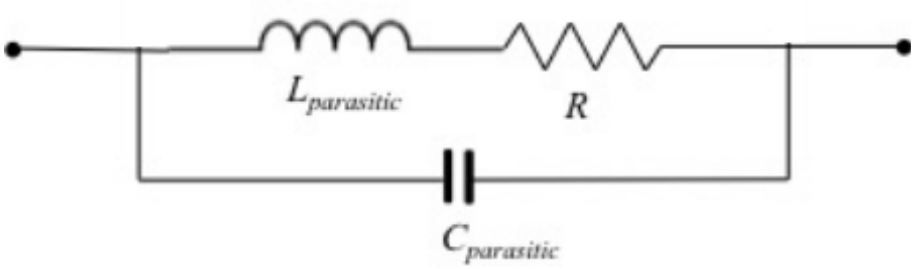


Fig. 5.24 Real model of a resistor[6].

Secondly, the chip of figure 5.27, with the resistor attached between the pads of both Correction electrodes, is measured following the Π model too as depicted in figure 5.28,

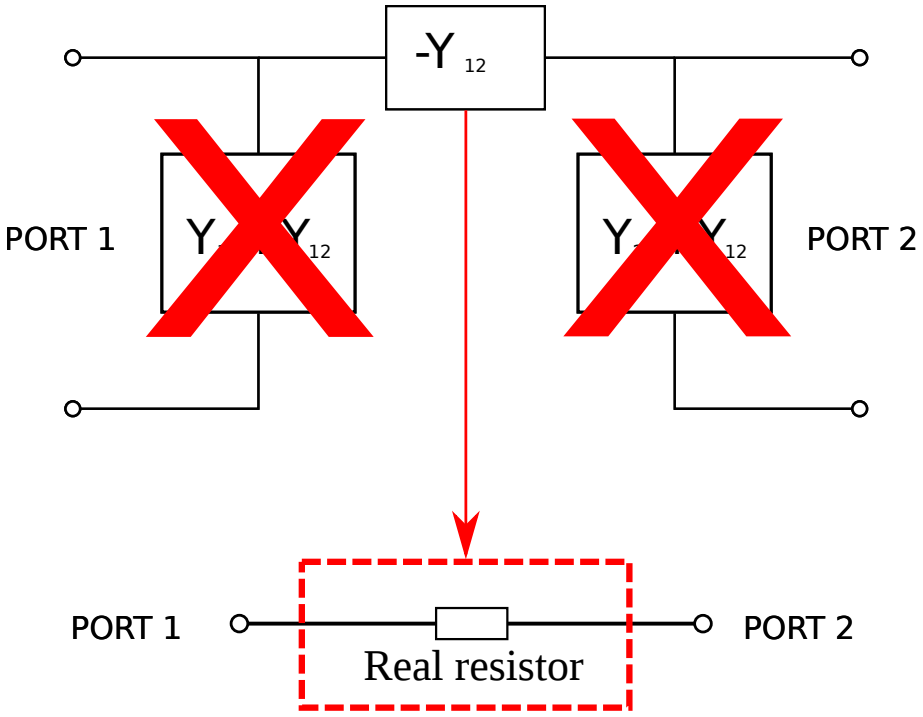


Fig. 5.25 Π model equivalent used for the measurement of the SMD resistor.

connecting the ports of the VNA to the pads of the Correction electrodes, and analysing the impedance of the coupling with the same fitting model of figure 5.24, that is, with the model of a real resistor. In this case, this fit, which is represented in figure 5.29, gives a value of $C_{parasitic}$ equal to the total capacitance of the resistor added to the capacitance of the chip.

Fig. 5.26 Resistor with two SMA connectors soldered.

The impedances of both measurements are represented in figure 5.30 and the results of the capacitance obtained from the fitting are listed in table 5.2. The capacitance added by

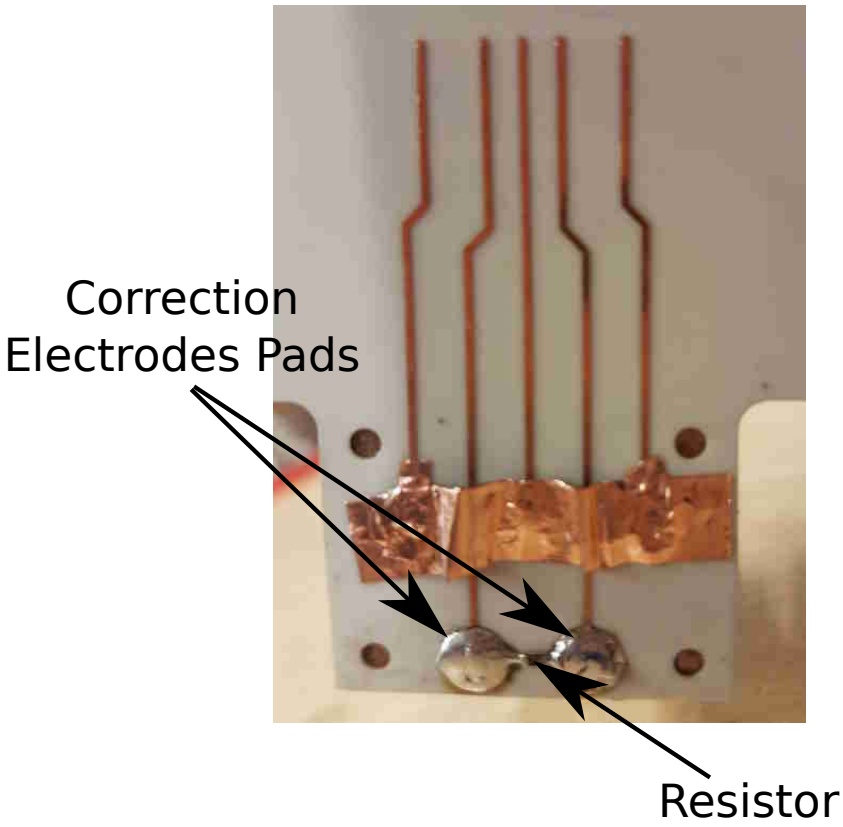


Fig. 5.27 Resistor placed between the pads of the Correction electrodes of the chip.

the resistor is only 0.07 pF and the total capacitance of the chip including the resistor is 0.17 pF.

Electrode	Capacitance (pF)	Error (pF)
Only resistor	0.07	0.02
Chip with resistor	0.17	0.0002

Table 5.2 Capacitances of the 24.8 kΩ resistor and coupling capacitance between the Correction electrodes of a P.W.Circuit chip with the 24.8 kΩ SMD resistor attached.

The procedure is repeated for another resistor of 50 kΩ from the same company. The results of this measurement are listed in table 5.3. These are similar to the results of the 24.8 kΩ resistor.

Electrode	Capacitance (pF)	Error (pF)
Only resistor	0.06	0.03
Chip with resistor	0.13	0.0003

Table 5.3 Capacitances of the 50 kΩ resistor and coupling capacitance between the Correction electrodes of a P.W.Circuit chip with the 50 kΩ SMD resistor attached.

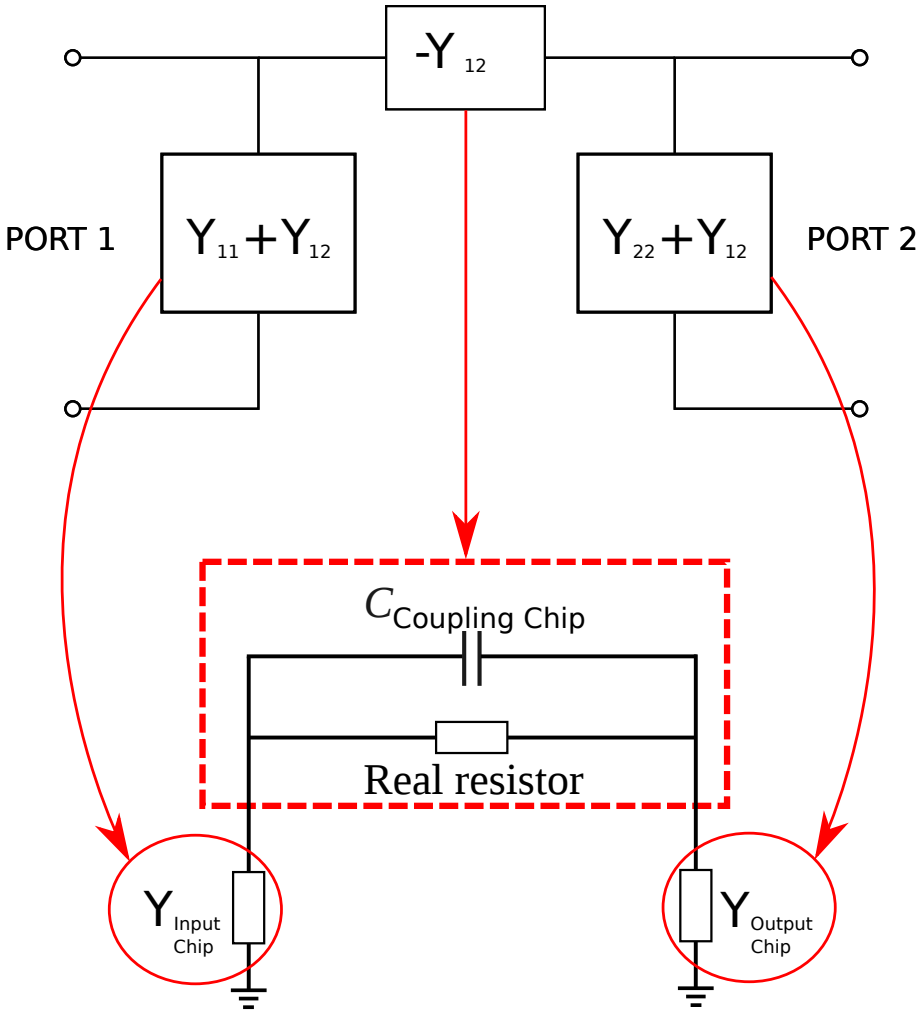


Fig. 5.28 Π model equivalent used for the measurement of the P.W.Circuit Chip with the SMD resistor attached.

The obtained results show that the capacitance of the chip is the limiting factor, since it is the element that adds most of the capacitive effect. Therefore, since the capacitance added by the resistor is small comparing to the capacitance of the rest of the system, the detection of the trapped electrons is possible.

A representation of a single trapped electron spectrum, generated by this equivalent circuit of figure 5.23 with the real parasitic values measured above, is shown in figure 5.31.a) for the case of 24.8 kΩ resistor and in figure 5.31.b) for the 50 kΩ resistor. It proves that the trapped electron is visible with both resistors.

5.3.4 The resistor as universal detector

In order to prove that different particles could be detected with the same resistor, the detection of a trapped proton has been simulated.

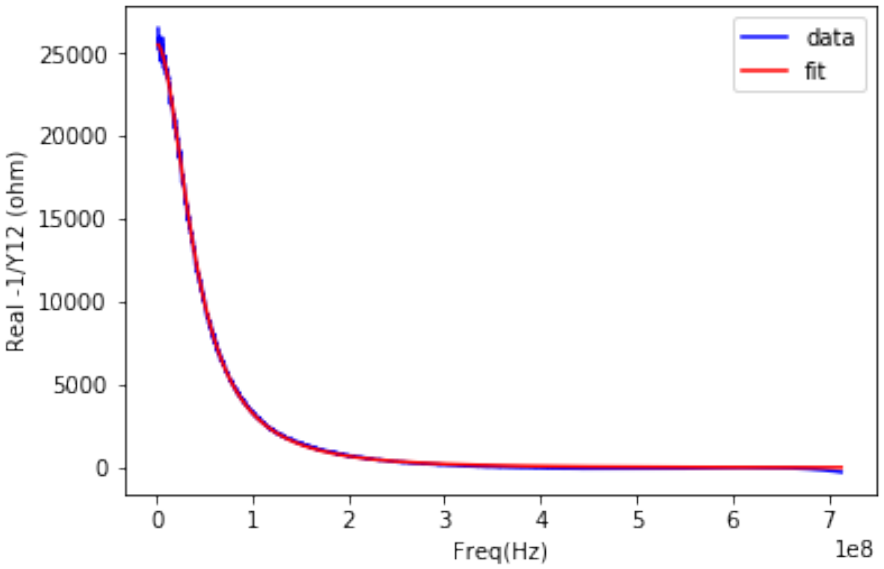


Fig. 5.29 Data and fit of a P.W.Circuit chip measurement with the VNA connected to both Correction electrodes and a 24.8 kΩ SMD resistor attached.

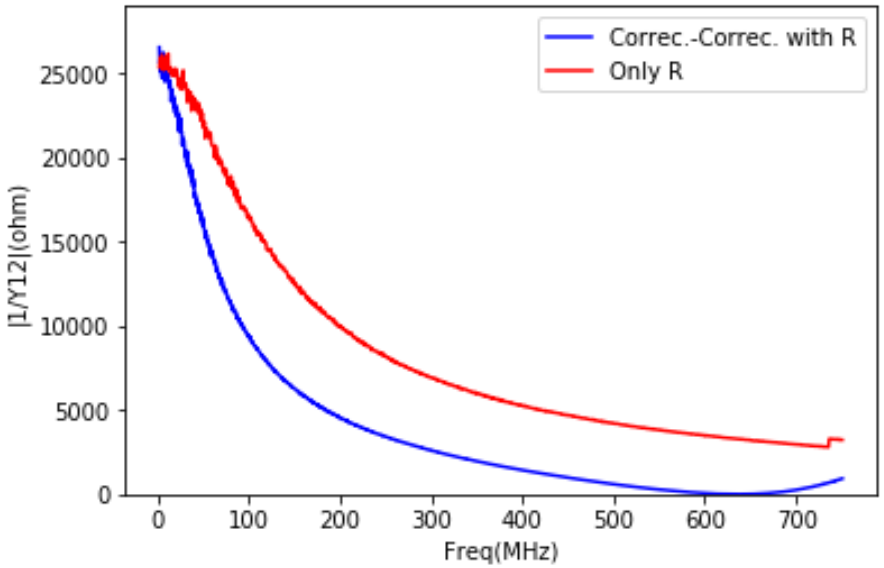


Fig. 5.30 Impedance of a SMD resistor of 24.8 kΩ of the company *Stackpole Electronics Inc.* (red line) and impedance of the coupling between Correction electrodes of a P.W.Circuit with the same resistor soldered between them (blue line).

A 500 kΩ resistor has been used in these simulations. As introduced in section 2.6, the width of the dip depends on the ratio q^2/m, which is lower in the case of protons comparing to electrons, since the mass of protons is bigger, but the absolute value of the charge is similar. However, attending to the simulation results, a resistor of 500 kΩ is enough to detect this particle. The results of this simulation are shown in figure 5.32.

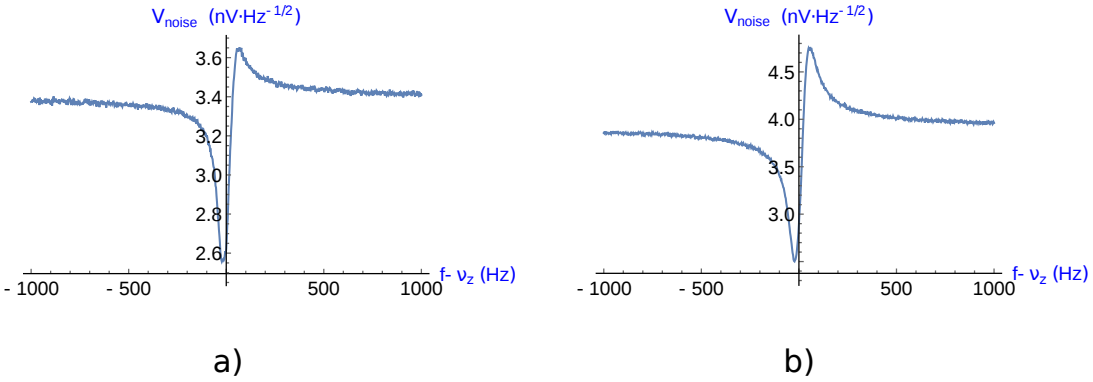


Fig. 5.31 Simulation of the detection of an electron with a a) 24.8 kΩ and b) 50 kΩ resistor, with the parasitic values measured in section 5.3.3 and the model of figure 5.23.

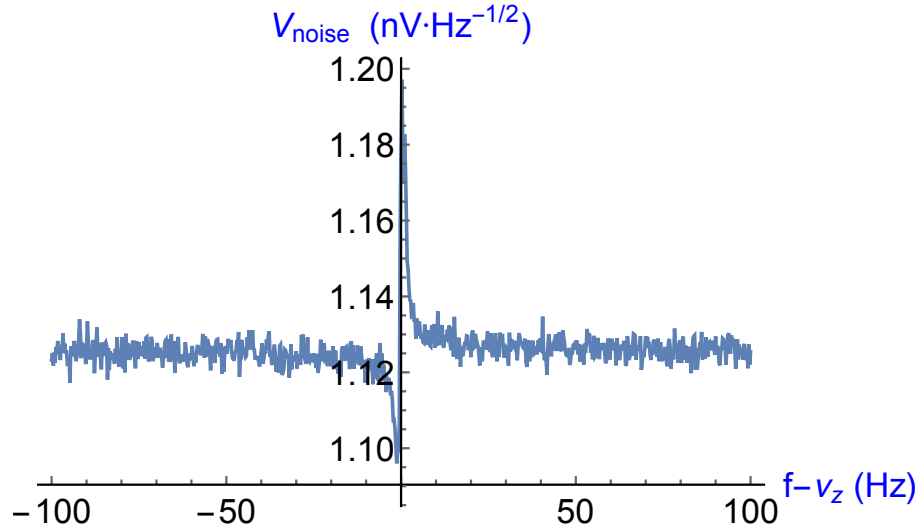


Fig. 5.32 Results of the simulation of a single proton detection with a 500 kΩ resistor.

5.3.5 Conclusion

The design of a broadband, universal and compact detection system, based on a single SMD resistor, has been introduced and the detection of different particles using it has been proved, if they have a reasonable q^2/m ratio. Although only the examples of a proton and an electron detection have been shown in this section, the system could detect different charged particles and it can be adapted for the detection of the ones with a lower q^2/m ratio by increasing the value of the resistor.

The design of a differential amplifier is still in progress and will be completed in the next weeks or months. It will be finally installed in the Geonium Chip experiment, replacing the current detection system based on a superconducting coil, and considerably reducing its size.

Chapter 6

Coupling electrons with microwave photons

As described in section 2.7, one of the main applications of the Geonium Chip is the nondemolition single microwave photon detection. A waveguide is required in order to guide the microwave photons into the cavity where the electron is trapped in order to be detected [13]. With this aim, an antenna will be installed inside the cryogenic chamber providing a higher coupling strength than the CPW line presented in [13]. This will be connected to the rest of the system with a coaxial cable that will transmit the photons from an external source to the antenna.

According to the description of section 2.7.3, the strength of the coupling depends on the distance between the trapped electron and the antenna. Since the height of the trapped electron y_0 can be tuned by changing the voltages of the electrodes, the distance between the electron and the antenna can be easily controlled, thus controlling very accurately the intensity of the coupling. Therefore, the photons could be absorbed by the electron, or emitted from it, from a position very close to the antenna, while the detection could take place from a different height with a more optimal potential.

With this antenna, the trapped electron could absorb or emit photons on demand. However, the antenna will introduce a perturbation in the potential, making it more anharmonic. Hence, the position and the dimensions of the antenna in the chamber need to be analysed in order to minimize the effect of this perturbation.

In this chapter, the electrostatic field created by different set-ups is studied in order to obtain the optimal configuration. Two different simulations are performed, a 2D

simulation with the FEMM software [66] and a 3D one with Elmer[62]. The results of the second one are more similar to the theoretical values provided in [93], therefore, this has been the software used in the analysis described in this chapter.

6.1 Coefficients analysis

The perturbation of the harmonicity of the trap potential is analysed using the coefficients described in equations 2.30 and 2.31.

C_{002} coefficient appears in the expression of the quadrupole potential ϕ_{quad}, as shown in equation 2.33, and the ratio between the axial frequency and energy $\Delta\nu_z/\Delta E_z$ depends on C_{004}, C_{012} coefficients, according to equation 2.36 and 2.37 [93]. The next most significant even anharmonicity is C_{006} [93]. Therefore, the variation of these four coefficients C_{002}, C_{004}, C_{006} and C_{012} presents the most important contribution to the perturbation of the trap potential and they are simulated and analysed for different set-ups.

C_{002}, C_{004}, C_{006} can be obtained by fitting the potential with the following expression

$$V(z) = C_{002}z^2 + C_{004}z^4 + C_{006}z^6, \tag{6.1}$$

while, according to equation 2.31, C_{012} could be related to C_{002} with the following equation

$$C_{012} = \frac{\partial C_{002}}{\partial y}. \tag{6.2}$$

6.2 2D Simulation of the perturbation of the antenna

A first test of a 2D simulator was performed for the case of the Geonium Chip with no added antenna, as this simulation is easier and less time consuming than a 3D one. However, it was dismissed after comparing with the results of the 3D simulation as the last ones agree better with the theoretical results [93]. The procedure and the results of this 2D simulation test are described in this section.

The 2D simulation is done with FEMM software [66], which simulates electrostatic field over a 2D plane.

The simulated region is the one between the chip and the cryogenic chamber at the middle point of the chip over the YZ plane. The dimensions of the chip and the chamber

are described in the software and also the materials of the objects and the space created between them, which is chosen as vacuum in this case. The model of the chip used for this simulation is similar to the P.W.Circuits chip described in section 4.4 and the voltages of every electrode are taken from the example proposed by Verdu [93]:

- The Ring electrode voltage is -1 V.
- The voltage of both Correction electrodes is -1.15 V.
- The voltage of the End-cap electrodes is -4 V.

The simulation results of figure 6.1 can be analysed in FEMM and the data of the potential along any line of the simulated plane can be exported.

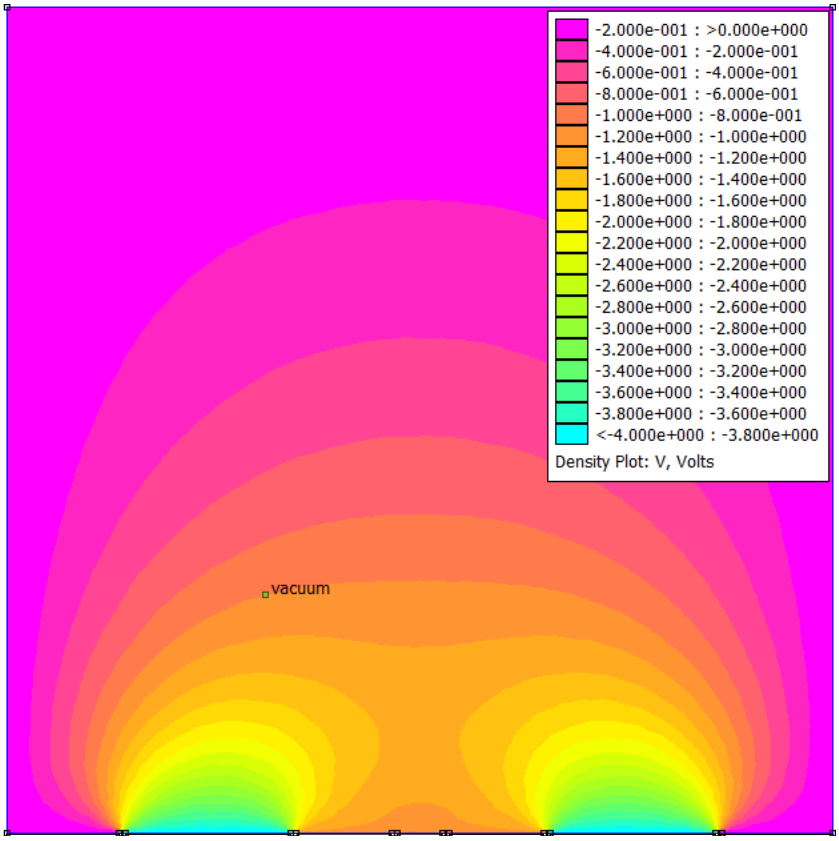


Fig. 6.1 Results of the FEMM simulation.

The height of the trapped electron is calculated as the minimum potential along the Y axis, which can be obtained from figure 6.2. The potential at this point is -1.36 V at 2.255 mm.

The potential along the Z axis is measured at different heights (figure 6.3) and the harmonic part of this potential, which is shown in figure 6.4 as a red line, is fitted following

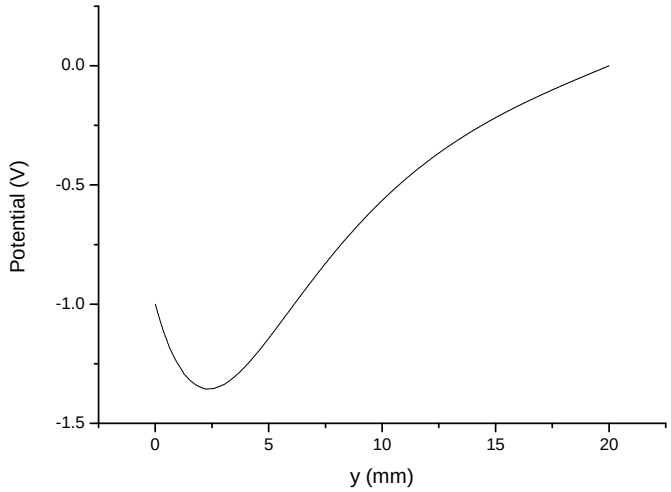


Fig. 6.2 Potential over the chip centre along the Y axis in the 2D simulation of the P.W.Circuit chip without antenna.

equation 6.1 to get the value of the C_{002}, C_{004} and C_{006} coefficients that appears in table 6.1. The value of these coefficients as a function of height is plotted in figure 6.5.

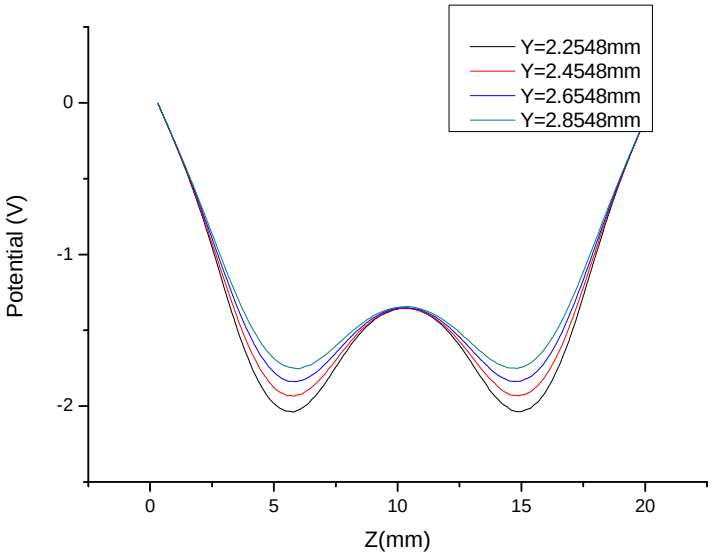


Fig. 6.3 Potential created over the chip along the Z axis at different heights in the 2D simulation of the P.W.Circuit chip without antenna.

The last coefficient C_{012} is calculated by fitting the line of C_{002}, using a linear fit where $C_{002} = C_{012} \cdot y$, following equation 6.2, and y being the coordinate in the Y axis. It is represented in figure 6.6 and the final result is $C_{012} = -0.01672 \pm 0.00461$.

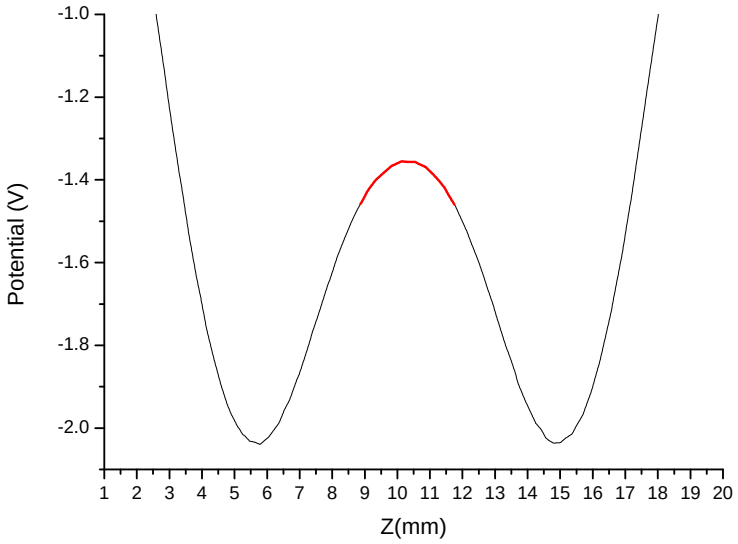


Fig. 6.4 Region where the potential is similar to a harmonic oscillator in the 2D simulation of the P.W.Circuit chip without antenna.

Y(mm)	C_{002}	C_{004}	C_{006}
2.255	0.04072	$-2.64 \cdot 10^{-4}$	$4.55 \cdot 10^{-7}$
2.455	0.04071	$-2.6395 \cdot 10^{-4}$	$4.55 \cdot 10^{-7}$
2.655	0.03667	$-2.468 \cdot 10^{-4}$	$4.65 \cdot 10^{-7}$
2.855	0.03092	$-2.027 \cdot 10^{-4}$	$3.59 \cdot 10^{-7}$

Table 6.1 Coefficients value obtained from the 2D simulation of the P.W.Circuit chip without antenna.

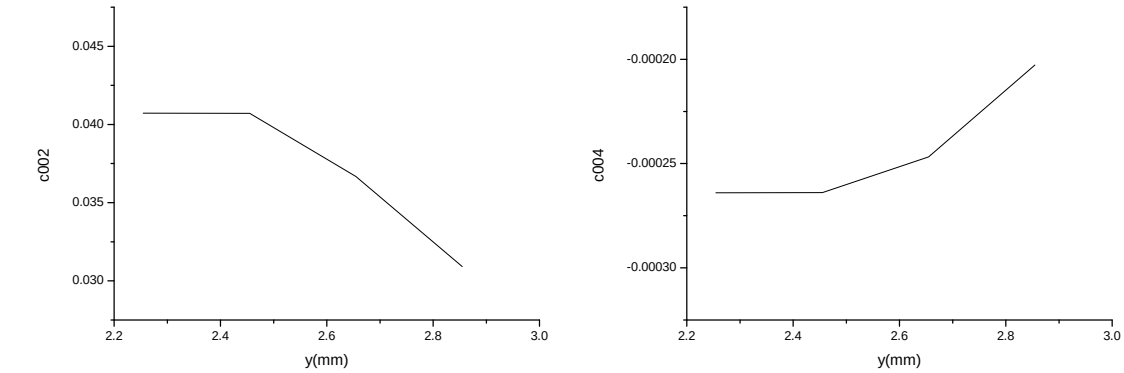
6.3 3D Simulation of the perturbation of the antenna

Three different set-ups are simulated: the P.W.Circuit chip without antenna and the same chip with antenna over the centre of the Ring electrode and on the top of the chamber.

The software used for the 3D simulation is Elmer. It is an open source multi-physical simulation software mainly developed by CSC-IT Center for Science [62]. Two external programs have been used to generate the mesh and to visualize the results of the simulation: Salome [8] and Paraview [57]. A description of both of them is provided in section 6.3.1.

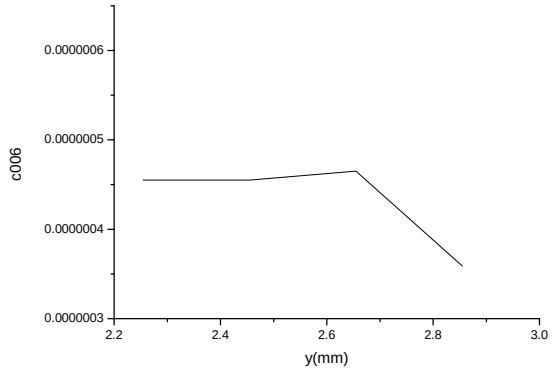
The model of the chip used for this simulation is similar to the P.W.Circuit chip described in 4.4 and the voltages for every electrodes are:

- Voltage of Ring electrode voltage: -1 V.
- Voltage of both Correction electrodes: -1.08017 V.



a)

b)



c)

Fig. 6.5 a)C_{002}, b)C_{004} and c)C_{006} coefficients obtained from the 2D simulation of the P.W.Circuit chip without antenna.

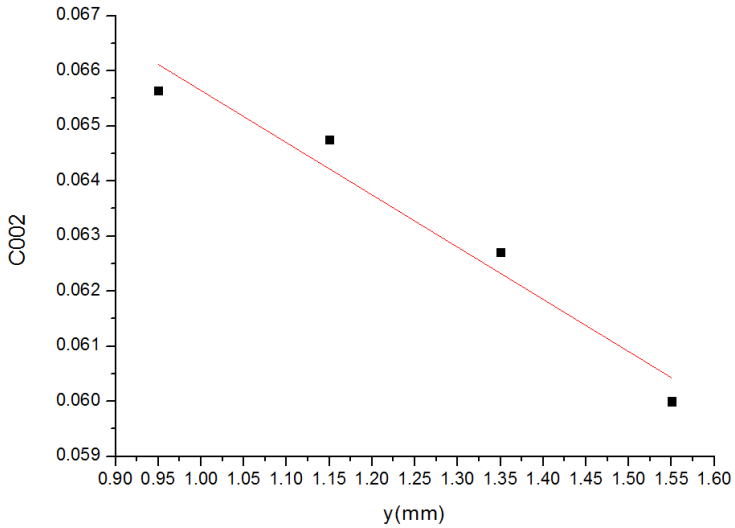


Fig. 6.6 Fitting of C_{012} from the data of C_{002} coefficient obtained from the 2D simulation of the P.W.Circuit chip without antenna.

- Voltages of both End-cap electrodes: -4.5 V.

The results of these simulations are obtained in collaboration with the PhD candidate Raquel Alvarez.

6.3.1 3D software and simulation description

The three different programs described in this section and used for this analysis are: Salome, to create the mesh, Elmer, which simulates the electrostatic fields, and Paraview in order to visualize easily the simulation results.

Salome

The mesh is done using the Salome software in the cavity created between the chip and the cryogenic chamber. The mesh size is specially small close to the chip, where the electron is trapped, as it is the interesting region to analyse.

The mesh is exported to Elmer as a UNV mesh file.

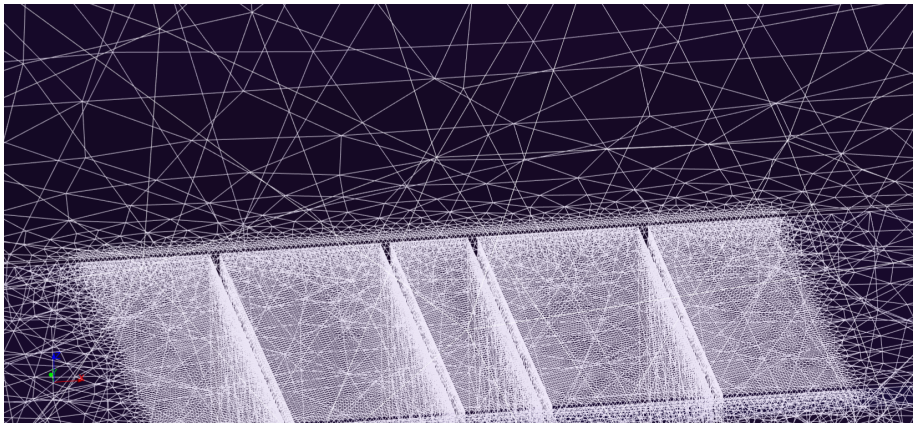


Fig. 6.7 Mesh of the cavity between the cryogenic chamber and the chip in Salome.

Elmer

In the Elmer simulation, air is consider as the material of the cavity and the boundary conditions are defined as the potential of each part of the system: the potential of Ring, Correction and End-caps electrodes and grounding the rest of the elements, that is, the walls of the chamber and the Ground Plane.

The results of this simulation are saved in a VTU file which can be opened with Paraview.

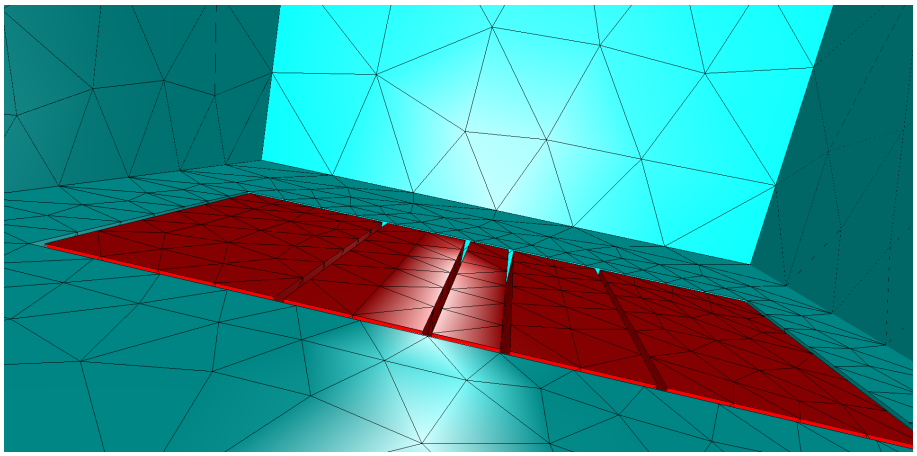


Fig. 6.8 Simulation of the potential in Elmer.

Paraview

The visualization using Paraview allows to analyse the potential results over different planes, plot graphs with the values of potential or export this data to be analysed with any software. In this case, the most interesting data to be analysed are the potential over the chip, where the electron is trapped, since the similarities of this potential in this region with a harmonic oscillator can be analysed attending to the coefficients described above.

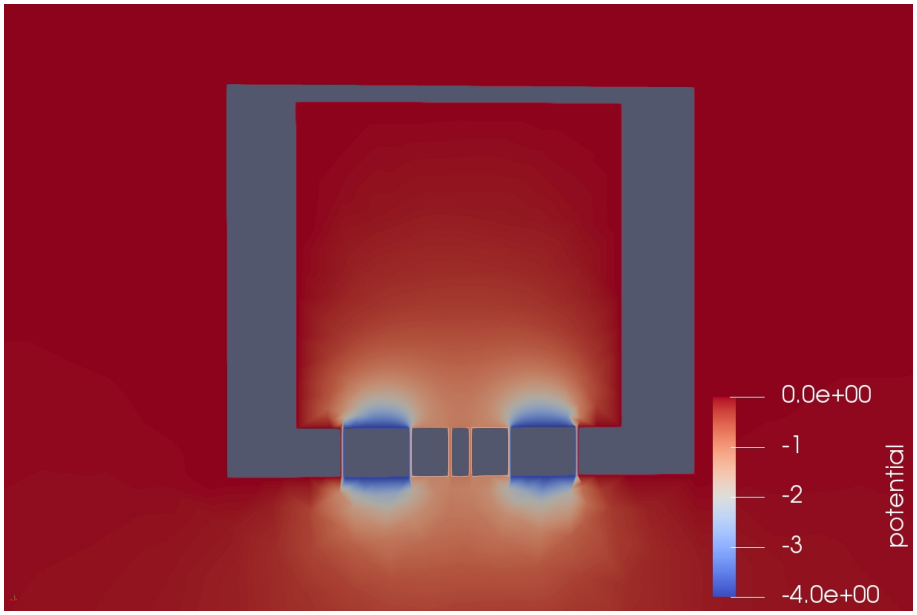


Fig. 6.9 Representation with Paraview of the results of the chip without antenna simulation.

6.3.2 3D simulation P.W.Circuit chip without antenna

The results presented in this section are the data obtained from the simulation without antenna on the chamber, that means, the unperturbed potential created by the chip. Figure 6.10 shows a picture of the simulated set-up.

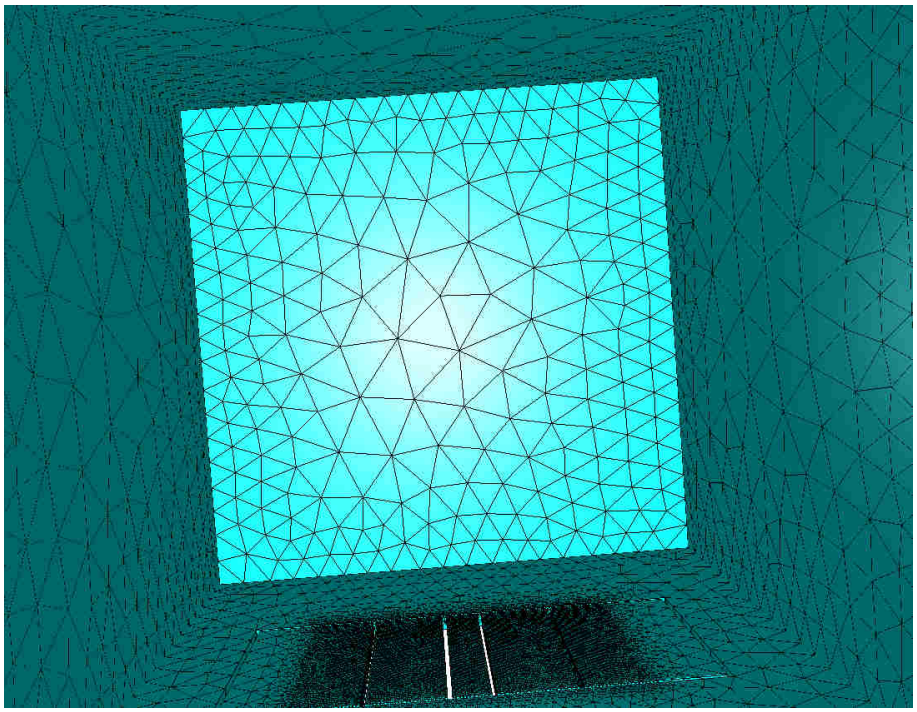


Fig. 6.10 3D simulation with Elmer of the P.W.Circuit chip and the chamber without antenna.

Y_0, the height of the trapped electron, is given by the minimum potential along the Y direction. Figure 6.11 shows the potential in the Y direction over the trap centre, above the middle point of the Ring electrode. The minimum value of the potential is -1.05372 V at Y_0 = 1.024 mm.

The value of this potential is obtained from the results of the simulation at different points near Y_0, as it is represented in figure 6.12, and the C_{002}, C_{004} and C_{006} coefficients for each of these heights are obtained from the fit of the harmonic part of each potential at these particular points (the fitted part of the potential, where it could be considered as harmonic, is shown as a red line in figure 6.13).

Finally, the values of these coefficients are listed in table 6.2 and the representation of it as a function of the height y is shown in figure 6.14.

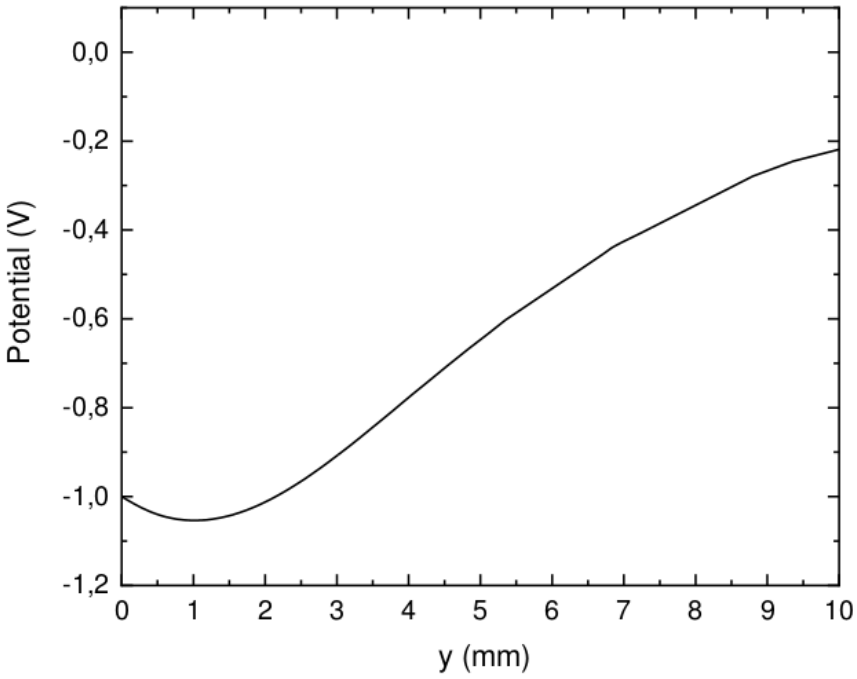


Fig. 6.11 Potential over the chip centre along the Y axis in the 3D simulation of the P.W.Circuit chip without antenna.

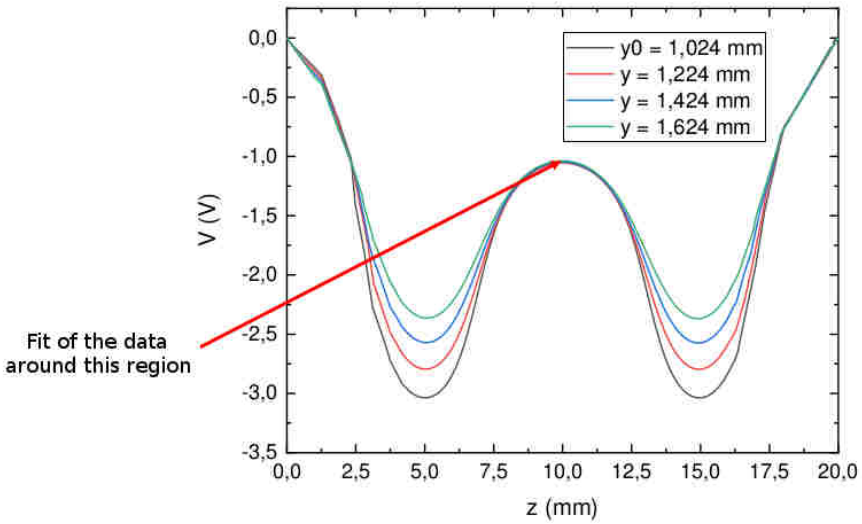


Fig. 6.12 Potential created over the chip along the Z axis at different heights in the 3D simulation of the P.W.Circuit chip without antenna.

Attending to equation 6.2, the C_{012} coefficient could be calculated from the slope value of the representation of C_{002} for different heights, as shown in figure 6.14, fitting it as a linear function. The fit done with Origin gives a value of C_{012} = 0.00632.

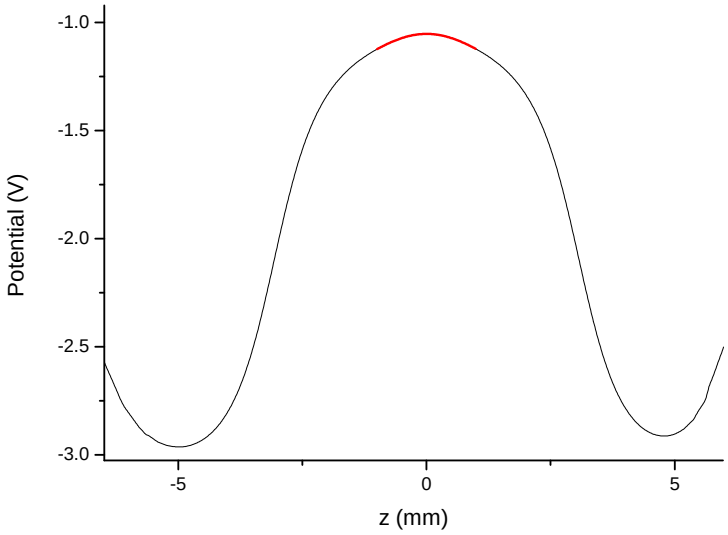


Fig. 6.13 Region where the potential is similar to a harmonic oscillator in the 3D simulation of the P.W.Circuit chip without antenna.

Y(mm)	C_{002}	C_{004}	C_{006}
1.024	-0.06644	0.00163	0.00265
1.224	-0.06631	$-2.55647 \cdot 10^{-4}$	-0.00247
1.424	-0.06581	$-3.18633 \cdot 10^{-4}$	-0.00223
1.624	-0.06232	-0.011	0.01256

Table 6.2 Coefficients value obtained from the 3D simulation of the P.W.Circuit chip without antenna.

6.3.3 3D Simulation with antenna on the chip

In order to simulate the chip with an antenna, the same procedure of section 6.3.2 is followed, with the same model of chip and chamber. In this case a cylindrical antenna is placed over the surface of the Ring electrode and held by the same chip. The simulated set-up is shown in figure 6.15.

The simulated antenna has 0.2 mm radius and 0.4 mm height as depicted in figure 6.16 and a voltage equal to the Ring electrode, that is, $V_{antenna}$ = -1 V.

The results of the potential along the Y axis is represented in figure 6.17, where the height of the lowest potential can be measured as Y_0 = 1.102 mm. For this particular value of y, the variation of the potential across the z axis is shown in figure 6.18. The points of interest are near z = 0 mm, since the anharmonicities are smaller in this region.

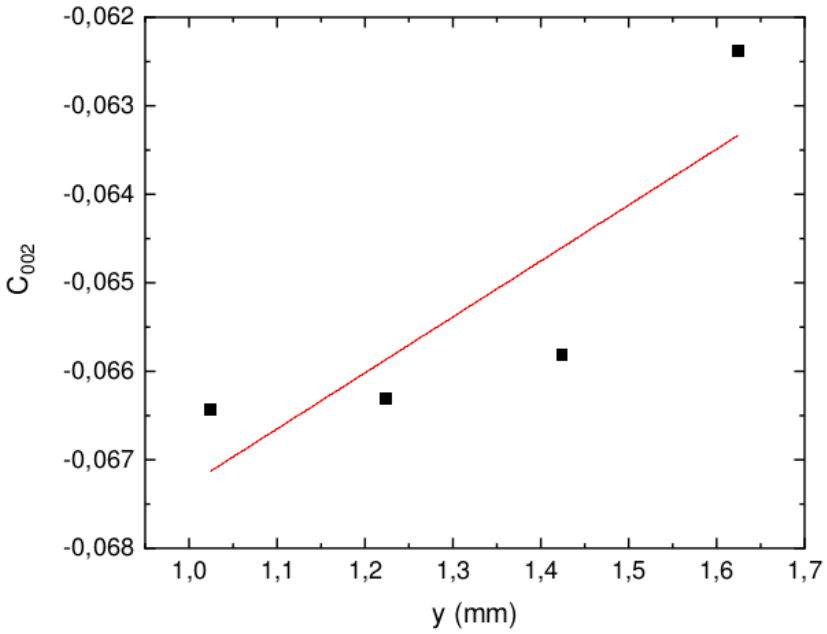


Fig. 6.14 Calculation of C_{012} coefficient for the simulation of the chip with no antenna.

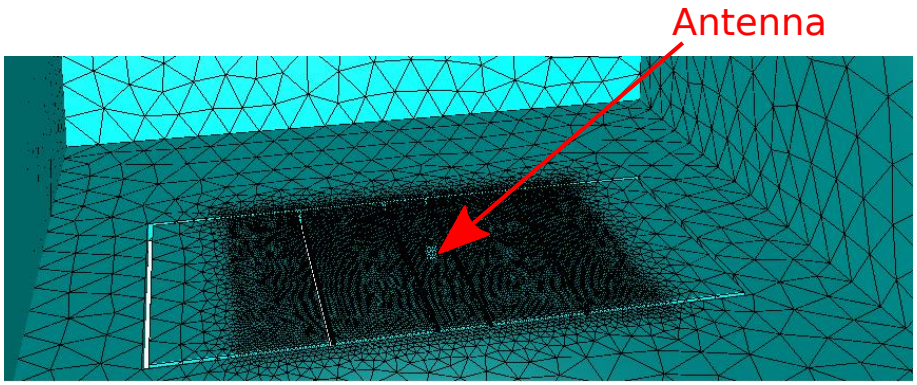


Fig. 6.15 Set-up of the P.W.Circuit chip and the chamber simulation using Elmer, with the antenna over the Ring electrode.

Following the same steps of the previous simulation without antenna, the C_{002}, C_{004} and C_{006} coefficients are analysed at four different heights near the point Y_0. The value of these coefficients as a function of y is listed in table 6.3. And following equation 6.2, the C_{012} coefficient is obtained from the fit of the C_{002} coefficient as C_{012} = 0.01539.

Y(mm)	C_{002}	C_{004}	C_{006}
1.102	-0.07363	0.00563	0.00205
1.202	-0.06884	-0.00199	0.0018
1.402	-0.0671	$-2.94635 \cdot 10^{-4}$	-0.00145
1.602	-0.06395	-0.0031	$5.66328 \cdot 10^{-4}$

Table 6.3 Coefficients value obtained from the 3D simulation of the P.W.Circuit chip with an antenna over the Ring.

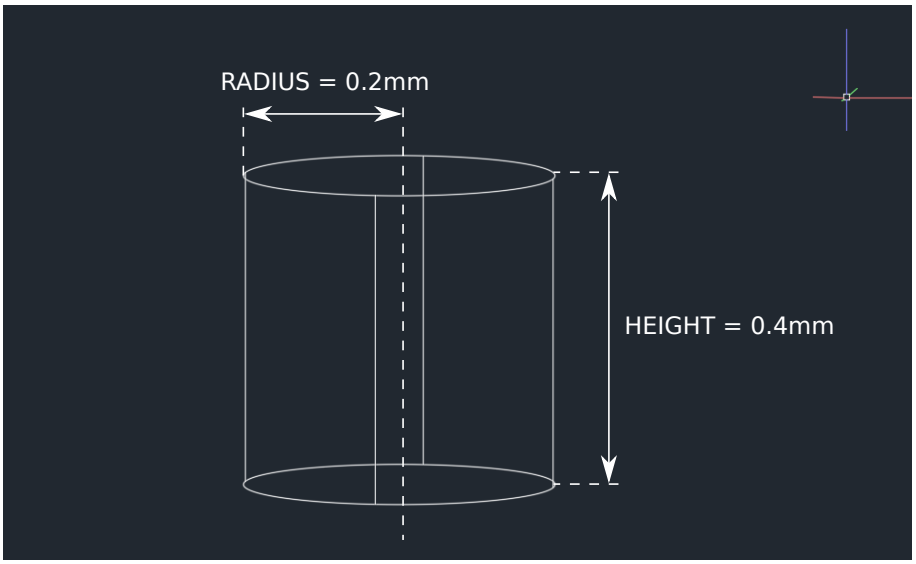


Fig. 6.16 Dimensions of the antenna simulated with Elmer.

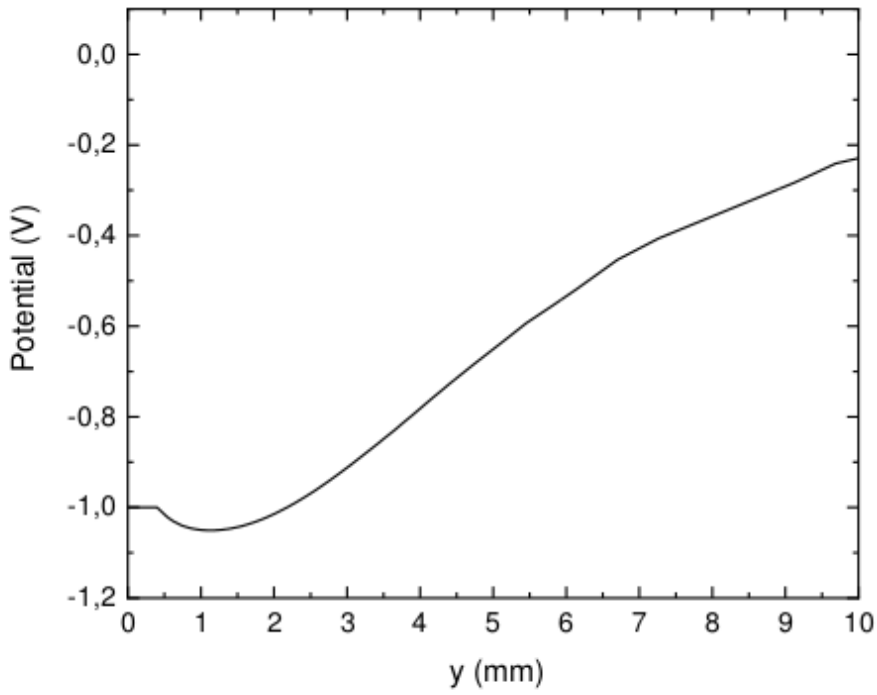


Fig. 6.17 Potential above the chip centre along the Y axis in the 3D simulation of the P.W.Circuit chip, with antenna over the Ring electrode. The minimum potential is at y=1.8832mm.

6.3.4 3D Simulation with antenna on the top of the chamber

For this simulation, the antenna is on the top of the chamber as shown in figure 6.19. In this case, the length of the antenna is 17 mm and 0.2 mm radius. The voltage of the antenna is 0 V, which is equal to the voltage of the chamber.

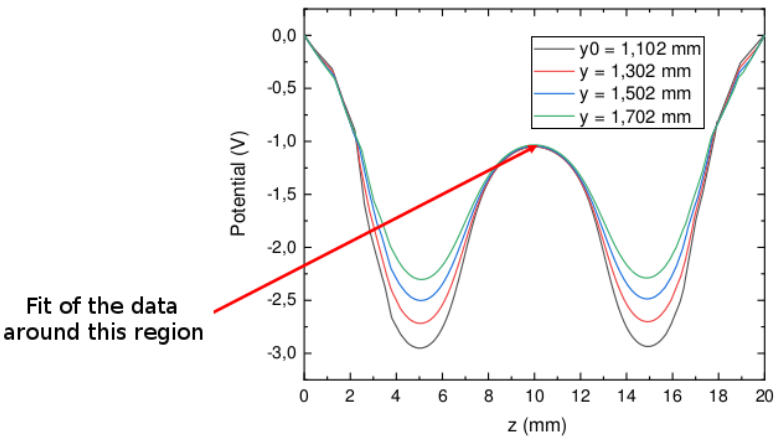


Fig. 6.18 Potential above the chip centre and along the Z axis in the 3D simulation of the P.W.Circuit chip, with antenna over the Ring electrode.

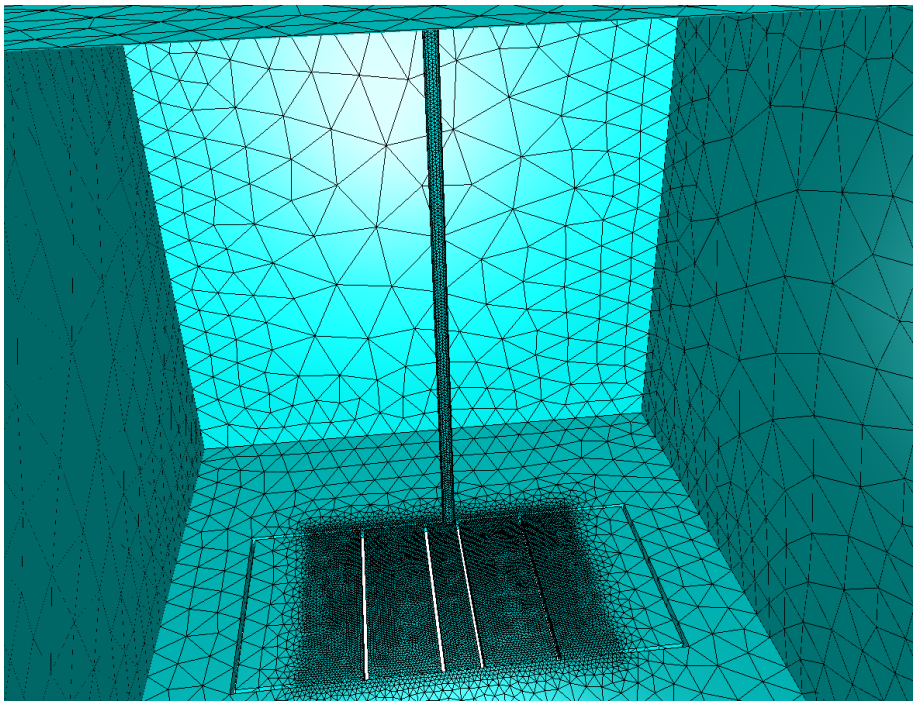


Fig. 6.19 Set-up of the simulation with the antenna placed on the top of the chamber above the centre of the Ring electrode.

The height of the lowest potential is Y_0 = 0.534, which, according to the representation of figure 6.20, has a potential of V_{min} = -1.015068 V. The results of the simulation along the Z axis for different heights in the region close to Y_0 is shown in figure 6.21.

The value of the coefficients, obtained with the same method used in previous sections, is listed in table 6.4. The value of C_{012}, calculated by fitting the results of the C_{002} coefficient as described in the previous section, is C_{012} = -0.00955.

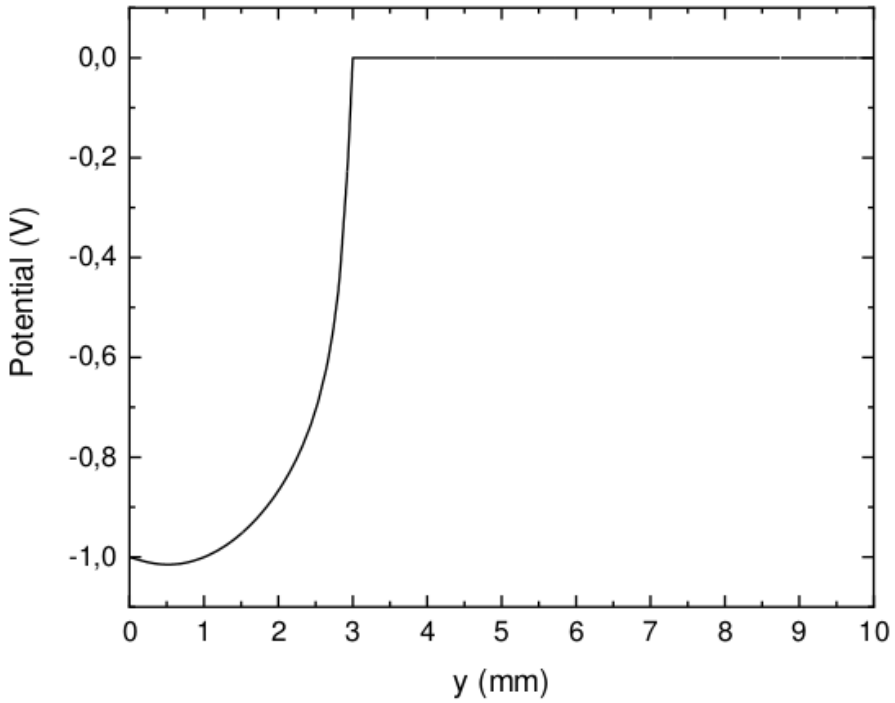


Fig. 6.20 Potential over the chip centre along the Y axis in the 3D simulation of the P.W.Circuit chip, with antenna on the top of the chamber.

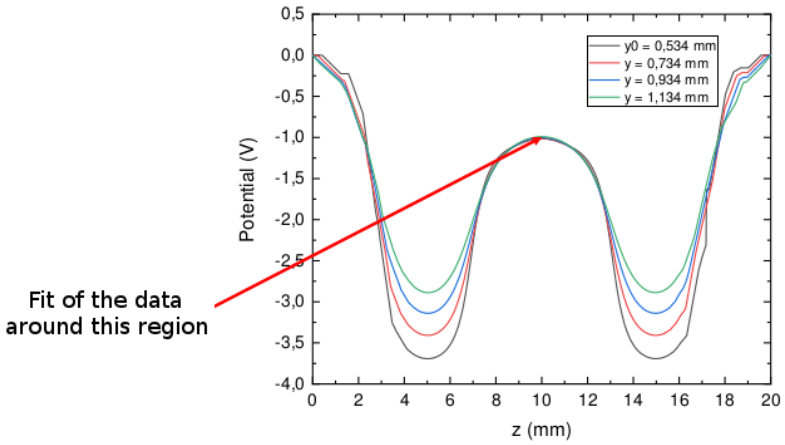


Fig. 6.21 Potential over the chip centre along the Z axis in the 3D simulation of the P.W.Circuit chip, with antenna on the top of the chamber.

Y(mm)	C_{002}	C_{004}	C_{006}
0.534	-0.07258	-0.00948	0.02174
0.734	-0.07332	0.00296	0.00269
0.934	-0.07482	0.00508	-0.00354
1.134	-0.07845	0.01383	-0.0187

Table 6.4 Coefficients value obtained from the 3D simulation of the P.W.Circuit chip, with an antenna on the top of the chamber.

6.4 Conclusion of the potential perturbation analysis

The results of the simulations show that the potential is not highly perturbed by introducing an antenna and the trap exists at a reasonable height. However, the design of the antenna on the top of the chamber implies more technical difficulties.

Therefore, the chosen model to be implemented in the Geonium Chip trap is the one with antenna on the Ring electrode.

This chapter represents only the first steps of the research to install an antenna that guides the microwave photons into the trapping region. However more progress needs to be done in the next years before the proposed solution can be finally implemented.

Chapter 7

Summary and outlook

7.1 Summary

The main achievements of this thesis are the characterization of the high frequency properties of the Geonium Chip trap and the development of a new detection system that replaces the big resonator with a small SMD resistor, thus, providing the trap with the capacity of detecting electrons at a broad range of frequencies. Additionally, the work in the laboratory and the improvements done in the Geonium Chip experiment have been thoroughly described. In conclusion, the thesis can be summarized in the following points:

Improvements in the set-up

A improved method of sealing the inner Cryogenic Chamber to the chip, pinch-off tube and window has been developed, removing the Epoxy and replacing it with indium, which is more resistant to cycles of expansion and contraction due to temperature changes, reducing the probability of leaks. With this improvement, some other processes, such as baking the chamber and optimizing the target where the electrons are ejected, have been introduced, increasing the photocurrent generated by the UV light beam. Finally, a new cooling system has been designed and installed, which reduces the heat supplied to the cryostat from the external electronic components, helping to reach lower temperatures.

HF Analysis of the microfabricated chip

The microfabricated chip presented some problems related to the high values of the parasitic components. A complete characterisation of the high frequency properties of this

chip has been thoroughly reported, concluding that the substrate material and the design of the chip increased the parasitic capacitance and resistance, deteriorating the resonance of the superconducting coil and making the detection of the trapped electron impossible.

Design and characterization of a new PCB chip

A new model of PCB chip was developed in order to solve the problems presented by the previous microfabricated one. It has been characterised and tested with a resonator. Its parasitic components have been proven to be within the required limits and, therefore, the chip can be used to trap. It has been installed in the experiment and is being used for the trapping attempts at the time of writing this thesis.

Detection system improvements: new resonators

New models of resonator have been proposed in order to reduce the size of the superconducting coil currently used in the experiment, which is one of the biggest devices of the system. It would reduce considerably the size of these experiments, which is one of the limiting factors in finding new uses and applications, and could work at highest frequencies that the current resonator.

Detecting the electrons with an SMD resistor

The revolutionary idea of using an SMD resistor as a detector has been introduced. It is placed between the Correction electrodes of the chip, replacing the big resonator. This new system has clear and significant advantages:

- The very big resonator is removed, thus, massively reducing the size of the experiment. The new system consists of a small SMD resistor integrated with the same chip of the trap, increasing slightly the area of it.
- While the resonator detects the trapped particles oscillating in a narrow range of frequencies close the the resonant frequency, the resistor provides a broad band detection, which is extremely useful for applications such as mass spectrometry.

This has been proven for the frequency of interest of the Geonium Chip experiment, that is, the axial frequency of the electron. However, it means that could detect other

lower frequencies, for example, the cyclotron frequency of a trapped proton, becoming a universal detector system.

Coupling the electron with external radiation: the principle of the microwave photon detection

Some simulations have been done to evaluate the effect of an antenna over the electrostatic fields of the trap. The decision of placing the antenna on the Ring electrode has been taken on the basis of these results.

Although these are only the initial steps of the new set-up development for the coupling of the external photons with the trapped electron, the obtained results are promising.

7.2 Outlook

Following the summary of the results and achievements of my research, this last section is dedicated to discuss the next steps and goals of the Geonium Chip experiment.

As I am writing this thesis, the attempts of trapping are taking place in the laboratory. It has been the main focus of our group and could be completed in the coming weeks. Therefore, the imminent goal is trapping and detecting a cloud of electrons with the current system, tuning the potentials of the trap and isolating one single electron. It will represent a milestone in the development of Penning traps since it would be the first trapping of a single electron with a planar, scalable and compact Penning trap.

The results obtained from the high frequency analysis and detailed in this thesis will be extremely important for the design of future generations of microfabricated Geonium Chip traps, with more accurate manufacturing techniques than PCB, in order to obtain a more precise trap and using new materials that meet the requirements. In the few next years a new research will need to be done, considering the data provided in this document, to optimize the chip for future applications.

Another major milestone will be reached with the design and testing of the proposed new detection system, which will need to be completely tested and installed in the trap. Due to its numerous advantages, it could revolutionise the way that charged particles are detected in Penning traps. In the case of the Geonium Chip, it will facilitate the implementation of some applications, for instance, mass spectrometry.

Finally, the first steps in the development of a set-up for the microwave photon detection have been presented. More research about this will be done in the coming months and years before the detection of such small energies can become a reality.

All these applications, and many others that have not been mentioned here, make the Geonium Chip a very versatile device with a promising future in the fascinating field of quantum technology, where this thesis aims to be a modest contribution.

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Appendix A

Electric fields in a CPW

The electric fields created by the CPW transmission line, similar to the one introduced in section 2.7, are given by [82, 13]. For a voltage of 1 V at the position of the trapped electron y_0 can be written as [13]

$$E_{CPW}^{even} = \frac{4}{\pi W}\sum_{n=1}^{\infty}\left[\frac{sin\left(n\pi\frac{W}{a}\right)sin\left(n\pi\frac{W+S}{a}\right)}{\sqrt{n^2+\frac{a^2}{\lambda_{MW}^2}-\frac{a^2\nu_{MW}^2}{c^2}}}exp\left(-\frac{2\pi y_0}{a}\sqrt{n^2+\frac{a^2}{\lambda_{MW}^2}-\frac{a^2\nu_{MW}^2}{c^2}}\right)\right] \quad \text{(A.1)}$$

$$E_{CPW}^{odd} = \frac{4}{\pi W}\sum_{n=1}^{\infty}\left[\frac{sin\left(\frac{2n+1}{2}\pi\frac{W}{a}\right)cos\left(\frac{2n+1}{2}\pi\frac{W+S}{a}\right)}{\frac{2n+1}{2}}exp\left(-\frac{2\pi y_0}{a}\sqrt{\left(\frac{2n+1}{2}\right)^2+\frac{a^2}{\lambda_{MW}^2}-\frac{a^2\nu_{MW}^2}{c^2}}\right)\right] \quad \text{(A.2)}$$

where S is the width of the central line of the CPW, W is the gap between this line and the Ground Plane and a is the total width of the chip, as shown in figure A.1. λ_{MW} and ν_{MW} are the wavelength and frequency of the microwave photon respectively.

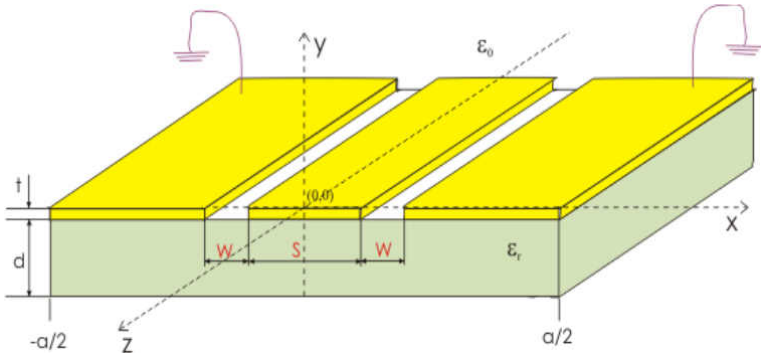

Fig. A.1 Dimensions of the CPW transmission line used in [13] to guide the microwave photons into the trapping region.

Appendix B

Basic concepts of high frequency analysis

B.1 Introduction to the high frequency analysis

This appendix presents the theory of the high frequency analysis of Transverse Electromagnetic (TEM) lines, which is a type of lines that supports the propagation of electromagnetic waves with the electromagnetic field vectors perpendicular to the direction of propagation.

Every TEM line has a terminal pair, similar to figure B.1, which allows us to define the voltage between the + and - conductor as [77]

$$V = \int_{+}^{-} \bar{E} \cdot d\bar{l} \tag{B.1}$$

integrating between the + and - conductor; and the current on the + conductor as

$$I = \oint_{C^+} \bar{H} \cdot d\bar{l} \tag{B.2}$$

where C^+ represents a contour around the + conductor [77].

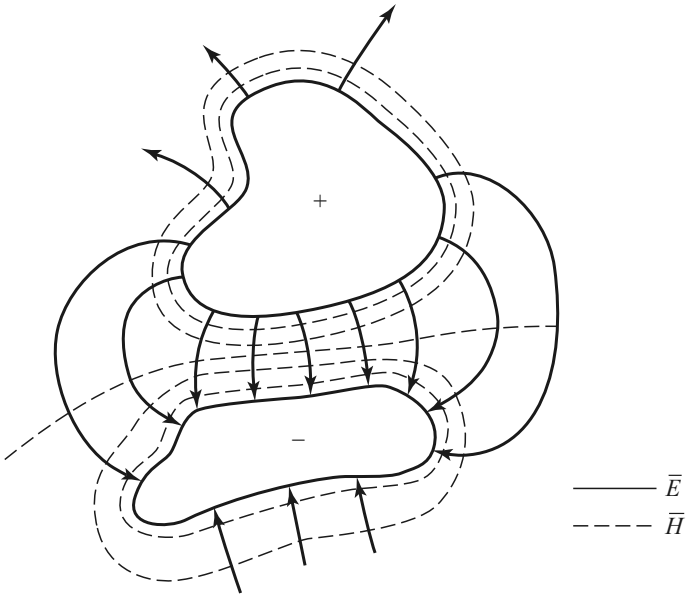

Fig. B.1 Electric and magnetic fields in a two-conductors TEM line [77].

The transverse fields of equations B.1 and B.2 are [77]

$$\bar{E}_t(x,y,z) = \frac{\bar{e}(x,y)}{C_1}\left(V^+ e^{-j\beta z} + V^- e^{j\beta z}\right) \tag{B.3}$$

$$\bar{H}_t(x,y,z) = \frac{\bar{h}(x,y)}{C_2}\left(I^+ e^{-j\beta z} + I^- e^{j\beta z}\right) \tag{B.4}$$

where $\bar{e}$ and $\bar{h}$ are the transverse field variation of the mode and the constants $C_1 = \frac{V_+}{A_+} = \frac{V_-}{A_-}$ and $C_2 = \frac{I_+}{A_+} = \frac{I_-}{A_-}$, A_+ and A_- being the field amplitudes of the travelling waves [77]. Thus, the voltage and current waves can be defined as [77]

$$V(z) = V^+ e^{-j\beta z} + V^- e^{j\beta z} \tag{B.5}$$

and

$$I(z) = I^+ e^{-j\beta z} + I^- e^{j\beta z}. \tag{B.6}$$

And the characteristic impedance of this system is [77]

$$Z_0 = \frac{V^+}{I^+} = \frac{V^-}{I^-} = \frac{C^1}{C^2}. \tag{B.7}$$

B.2 Scattering, impedance and admittance matrices

The scattering, impedance and admittance matrices can be defined in terms of the total voltage and current. Considering the N-port microwave system of figure B.2, the total voltage V_n and the total current I_n for the nth terminal, according to equations B.5 and B.6 with z = 0, are [77]

$$V_n = {V_n}^+ + {V_n}^- \tag{B.8}$$

and

$$I_n = {I_n}^+ + {I_n}^-. \tag{B.9}$$

B.2.1 Impedance and admittance matrices

Using the values of the total voltage and current of equations B.8 and B.9, the impedance and admittance matrices are defined as

$$\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} & \dots & Z_{1N} \\ Z_{21} & & & Z_{2N} \\ \vdots & & & \vdots \\ Z_{N1} & Z_{N2} & \dots & Z_{NN} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{pmatrix} \tag{B.10}$$

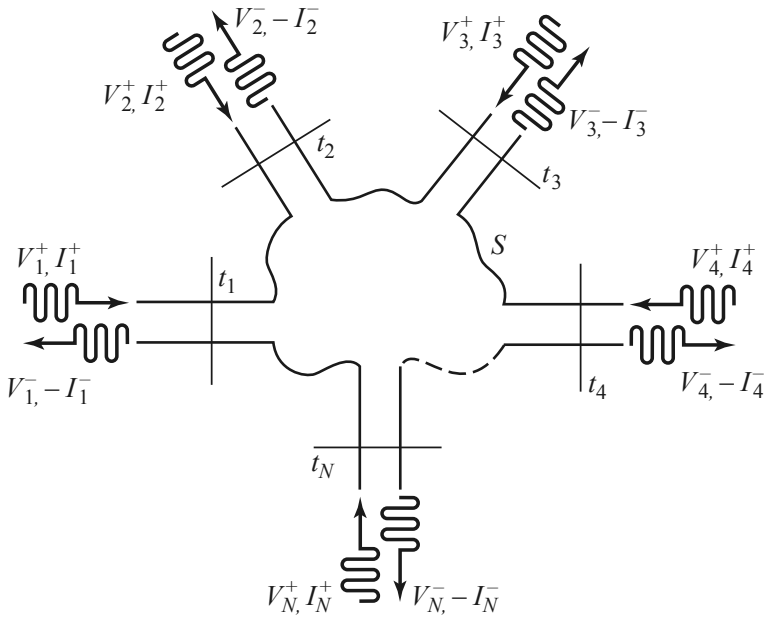

Fig. B.2 N-port microwave network [77].

and

$$\begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} & \dots & Y_{1N} \\ Y_{21} & & & Y_{2N} \\ \vdots & & & \vdots \\ Y_{N1} & Y_{N2} & \dots & Y_{NN} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{pmatrix}, \tag{B.11}$$

where the elements of the Z and Y matrices are

$$Z_{ij} = \left. \frac{V_i}{I_j} \right|_{I_k=0 \;\; for \;\; k \neq j} \tag{B.12}$$

and [77]

$$Y_{ij} = \left. \frac{I_i}{V_j} \right|_{V_k=0 \;\; for \;\; k \neq j}. \tag{B.13}$$

Following the previous equations, it is obvious that the impedance (or admittance) matrix, can be calculated as the inverse of the admittance (or impedance) matrix [77]

$$[Y] = [Z]^{-1}. \tag{B.14}$$

B.2.2 Scattering matrices

The scattering matrices are defined using the values of the voltage wave incident on port n (V_n^+) and the voltage wave reflected from port n (V_n^-) as

$$\begin{pmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & \dots & S_{1N} \\ S_{21} & & & S_{2N} \\ \vdots & & & \vdots \\ S_{N1} & S_{N2} & \dots & S_{NN} \end{pmatrix} \begin{pmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{pmatrix}, \tag{B.15}$$

where the scattering matrix elements are [77]

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+=0 \;\; for \;\; k \neq j}. \tag{B.16}$$

B.2.3 Conversion between scattering and impedance and admittance parameters in two-ports networks

The conversion between different parameters can be calculated from the equations of the sections B.2.1 and B.2.2. The simplest case and the one that we will use in our measurements is the two-ports network [77], that is, a network with only two ports, named as port 1 and port 2 as shown in figure B.3.

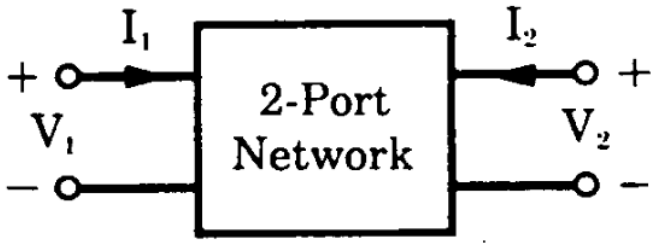

Fig. B.3 2-port microwave network [89].

The expression that converts from scattering to admittance and impedance parameters are:

- Conversion from scattering to admittance parameters [77]:

$$Y_{11} = Y_0 \frac{(1 - S_{11})(1 + S_{22}) + S_{21}S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}} \tag{B.17}$$

$$Y_{12} = Y_0 \frac{-2S_{12}}{(1+S_{11})(1+S_{22}) - S_{21}S_{12}} \tag{B.18}$$

$$Y_{21} = Y_0 \frac{-2S_{21}}{(1+S_{11})(1+S_{22}) - S_{21}S_{12}} \tag{B.19}$$

$$Y_{22} = Y_0 \frac{(1+S_{11})(1-S_{22}) + S_{21}S_{12}}{(1+S_{11})(1+S_{22}) - S_{21}S_{12}} \tag{B.20}$$

- Conversion from scattering to impedance parameters [77]:

$$Z_{11} = Z_0 \frac{(1+S_{11})(1-S_{22}) + S_{21}S_{12}}{(1-S_{11})(1-S_{22}) - S_{21}S_{12}} \tag{B.21}$$

$$Z_{12} = Z_0 \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{21}S_{12}} \tag{B.22}$$

$$Z_{21} = Z_0 \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{21}S_{12}} \tag{B.23}$$

$$Z_{22} = Z_0 \frac{(1-S_{11})(1+S_{22}) + S_{21}S_{12}}{(1-S_{11})(1-S_{22}) - S_{21}S_{12}} \tag{B.24}$$

B.2.4 Equivalent circuits for Y and Z parameters in a two port network

The transmitted and reflected waves are represented by scattering parameters. In the signal flow graph of figure B.4 each port i has two nodes: a_i, representing the input wave and b_i, the reflected wave from this particular port. The parameter S_{11}, which represents the part of the input wave of port 1 reflected to the same port, will be modelled as the part of a_1 transmitted to b_1; The part of a_1 transmitted to b_2 is represented by S_{21}; and, symmetrically, S_{22} and S_{12} are the parts of a_2 transmitted to b_2 and b_1 respectively [77, 9].

Considering that the network is reciprocal—it means that $Z_{12} = Z_{21}$ and $Y_{12} = Y_{21}$—, the Z parameters can be modelled as it is shown in figure B.5, using a T network where the values of the impedances are Z_{12}, $Z_{11} - Z_{12}$ and $Z_{22} - Z_{12}$. Equivalently, the Y parameters can be represented as a Π network, with the values for the admittances equal to Y_{-12}, $Y_{11} + Y_{12}$ and $Y_{22} + Y_{12}$ [77, 9].

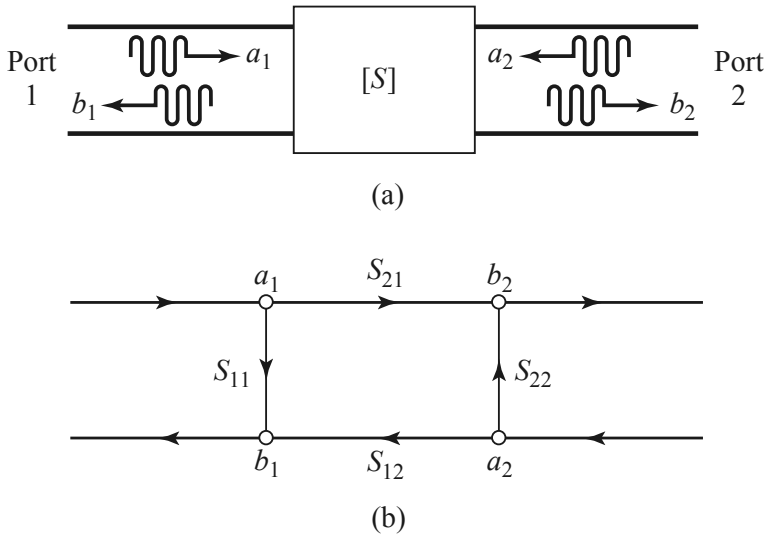

Fig. B.4 a) Incident waves a_1 and a_2 and reflected waves b_1 and b_2. b) Signal flow diagram in a two port network [77].

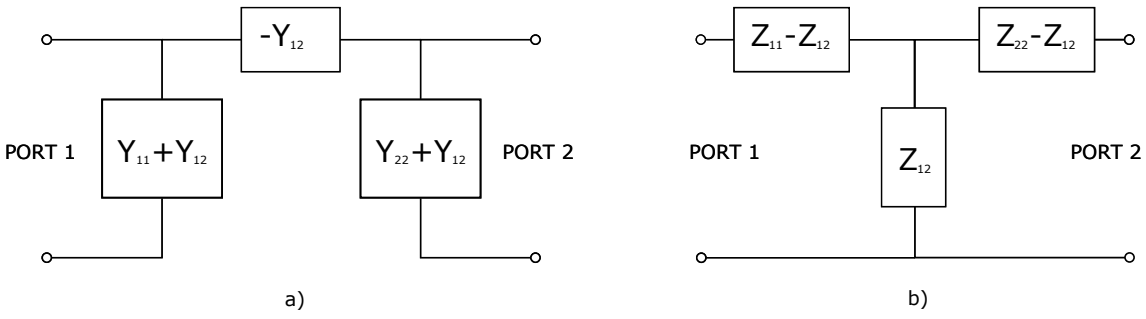

Fig. B.5 a) Π network. Equivalent circuit for the Y parameters. b) T network. Equivalent circuit for the Z parameters [77].

Appendix C

High frequency measurements of the P.W.Circuit chip with crimped SMA connectors

C.1 Set-up of the measurements

Unlike the set-up described in chapter 4, in the set-up the SMA connectors are not soldered to the chip. The VNA is connected to the chip using SMA connectors crimped to some terminals that are attached to the chip with nylon screws, as shown in figure C.1.

This method was finally dismissed as it was not totally robust, since the small variation in the position of the connectors would perturb the measurement. However, it is still interesting to observe the results, therefore it has been included in this appendix.

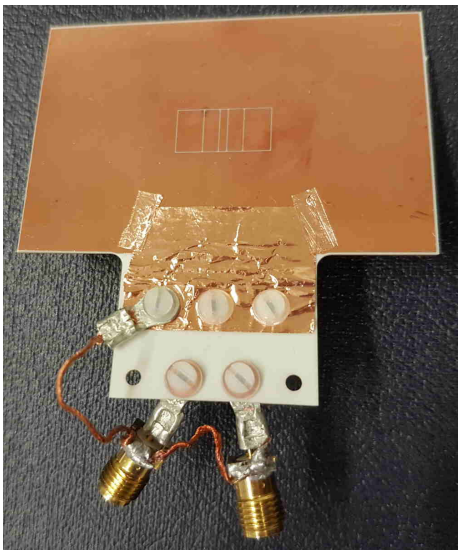

Fig. C.1 Set-up of the PWCircuit chip measurement. The VNA is connected to the SMA that appears in the picture.

C.2 Measurement of P.W.Circuit chip with the Pi network model

This chip is measured following the Π network model described in figure 4.2.2 with three different set-ups: 1) connecting to ground the Ground Plane of the chip and every electrode that is not being measured, 2) connecting to ground only the Ground Plane and side electrodes, but not the rest of the electrodes that are floating, and 3) not connecting any part of the chip to ground, but every part, apart from the electrodes that are being measured, is floating.

The results of these measurements are shown in figure C.2 and tables C.1, C.2 and C.3. It is not possible to see clearly and fit a resonance for every connection, therefore some of the cells of the tables are empty. In the case of the table C.3, only the combination UE(upper End-cap)-UC(upper Correction) could be fitted.

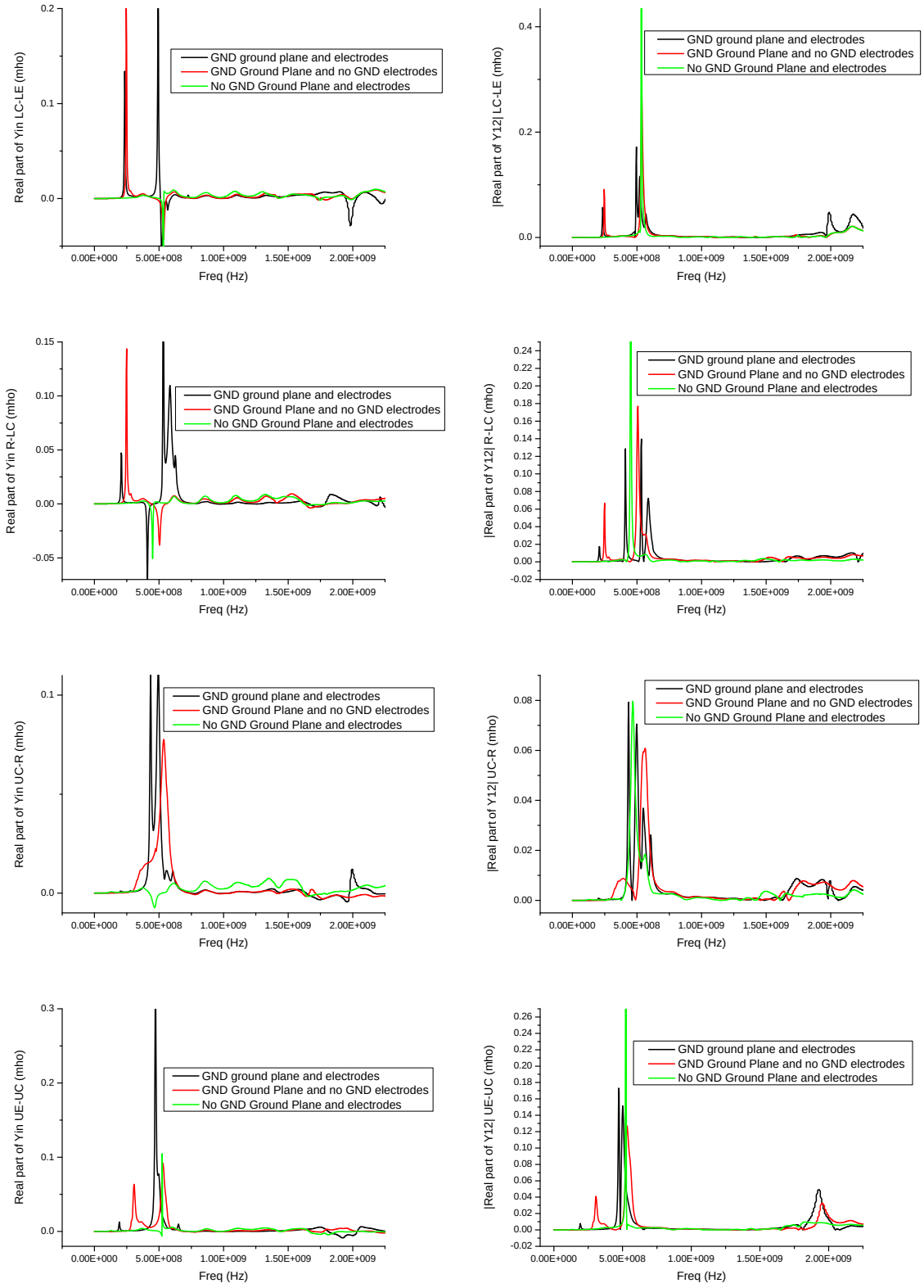

Fig. C.2 Symmetry between the Upper and Lower electrodes in the P.W.Circuit chip.

C.3 Measurement of P.W.Circuit chip with the T network model

The chip is measured with a T network set-up similar to the one of figure 4.2.3.

First resonance								
	UE-UC		UC-Ring		Ring-LC		LC-LE	
	Value	Error	Value	Error	Value	Error	Value	Error
Rs	77.453Ω		9.478Ω	0.365Ω	18.811Ω	0.159Ω	7.191Ω	0.279Ω
C	0.51pF	0.014pF	1.50pF	0.055pF	1.50pF	0.012pF	3.06pF	0.041pF
L	1.340μH	0.037μH	0.089μH	0.003μH	0.388μH	0.003μH	0.150μH	0.002μH

Second resonance								
	UE-UC		UC-Ring		Ring-LC		LC-LE	
	Value	Error	Value	Error	Value	Error	Value	Error
Rs	2.971Ω	0.063Ω	8.788Ω	0.219Ω	4.399Ω	0.639Ω	4.108Ω	3.346Ω
C	2.90pF	0.063pF	2.45pF	0.066pF	1.36pF	0.130pF	1.59pF	0.648pF
L	39.1nH	0.85nH	42.6nH	1.14nH	65.6nH	6.22nH	65.8nH	26.8nH

Third resonance								
	UE-UC		UC-Ring		Ring-LC		LC-LE	
	Value	Error	Value	Error	Value	Error	Value	Error
Rs					9.420Ω	0.207Ω		
C					2.02pF	0.039pF		
L					36.8nH	0.07nH		

Table C.1 Results of the measurement with the set-up 1 with Ground Plane and the rest of electrodes connected to GND.

First resonance								
	UE-UC		UC-Ring		Ring-LC		LC-LE	
	Value	Error	Value	Error	Value	Error	Value	Error
Rs	15.801Ω	0.550Ω	13.231Ω	0.084Ω	6.532Ω	0.225Ω	4.334Ω	0.066Ω
C	2.38pF	0.080pF	2.90pF	0.068pF	3.08pF	0.066pF	3.61pF	0.117pF
L	113nH	3.78nH	30.6nH	0.71nH	134nH	2.87nH	115nH	3.53nH

Second resonance								
	UE-UC		UC-Ring		Ring-LC		LC-LE	
	Value	Error	Value	Error	Value	Error	Value	Error
Rs	11.129Ω	0.259Ω						
C	1.87pF	0.038pF						
L	47.8nH	0.97nH						

Table C.2 Results of the measurement with the set-up 2 with Ground Plane and side electrodes connected to GND, but the rest of the electrodes floating.

The results obtained with this measurement are shown in figure C.3 and table C.4. Although there are three repetitions of the measurements in the graphs of figure C.3, the table lists only the average of the three values.

UE-UC						
	First Resonance		Second Resonance		Third Resonance	
	Value	Error	Value	Error	Value	Error
Rs	897.30Ω	37.75Ω	262.42Ω	8.28Ω	10.26Ω	0.7$\mu\Omega$
C	0.345pF	0.014pF	0.473pF	0.102pF	0.127pF	
L	4.33μH	0.18μH	0.39μH	0.008μH	0.73μH	

Table C.3 Results of the measurement with the set-up 3 with no part of the chip connected to ground.

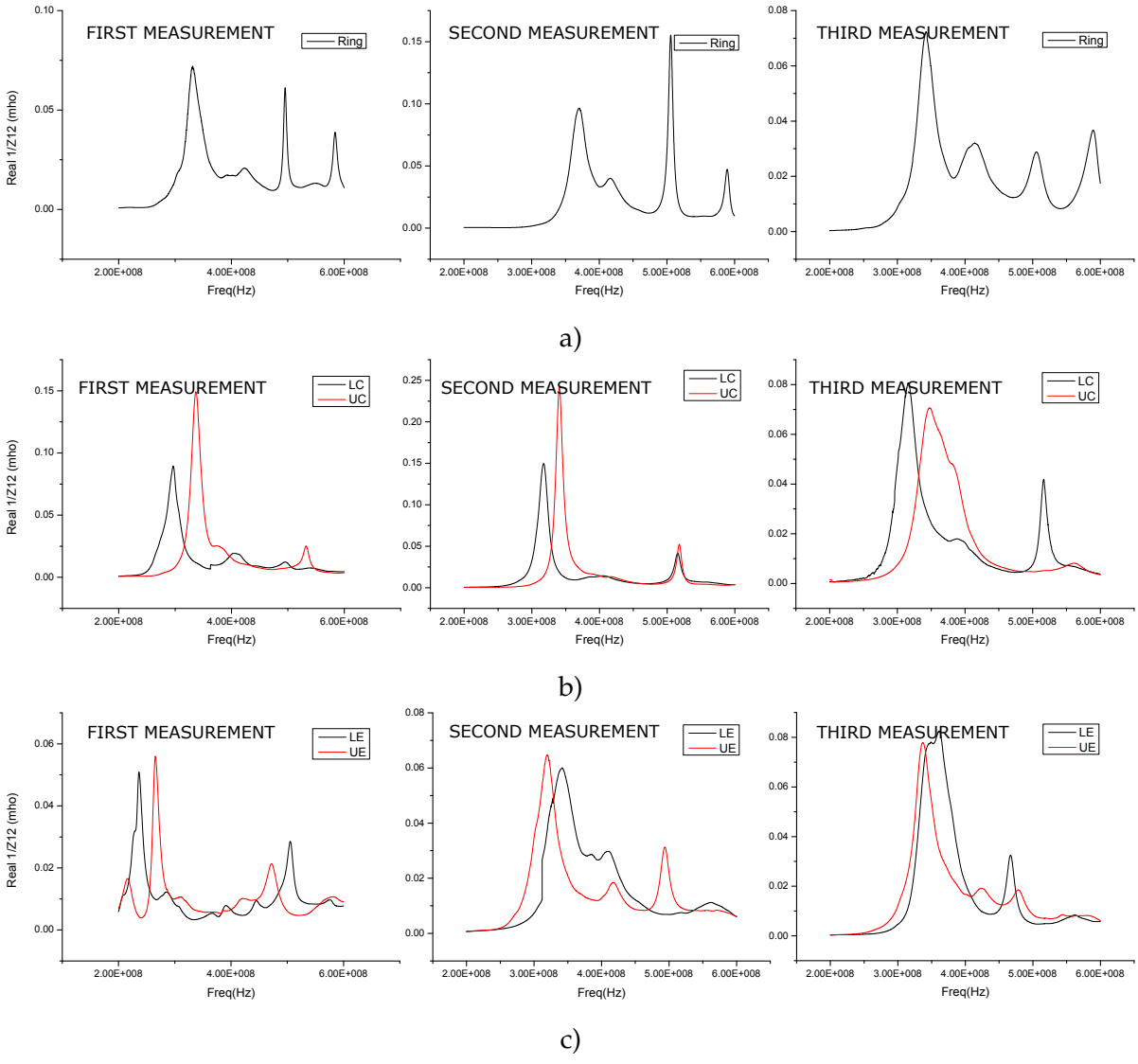

Fig. C.3 Results of the measurements of P.W.Circuit chip using T network model from the a) Ring electrode; b) Correction electrodes; c) End-cap electrodes.

Ring	1st resonance		2nd resonance		3rd resonance		4th resonance	
	Value	Error	Value	Error	Value	Error	Value	Error
Capacitance (pF)	3.38	0.009	1.82	0.006	0.69	0.003	0.29	0.002
Resistance (Ω)	12.76		31.56		19.37		24.63	
Inductance (nH)	60.12	0.02	78.27	0.02	127.18	0.06	181.12	0.14

Upper Correction	1st resonance		2nd resonance	
	Value	Error	Value	Error
Capacitance (pF)	4.268	0.007	0.297	0.001
Resistance (Ω)	8.30		22.70	0.11
Inductance (nH)	51.515	0.009	307.78	1.54

Lower Correction	1st resonance		2nd resonance	
	Value	Error	Value	Error
Capacitance (pF)	4.35	0.01	0.367	0.002
Resistance (Ω)	10.07		24.11	
Inductance (nH)	59.76	0.15	258.24	1.39

Upper End-cap	1st resonance		2nd resonance	
	Value	Error	Value	Error
Capacitance (pF)	3.27	0.008	0.51	0.002
Resistance (Ω)	15.44		39.69	
Inductance (nH)	60.79	0.16	220.08	1.00

Lower End-cap	1st resonance		2nd resonance	
	Value	Error	Value	Error
Capacitance (pF)	4.48	0.01	0.48	0.003
Resistance (Ω)	15.99		33.92	
Inductance (nH)	46.30	0.11	230.00	1.62

Table C.4 Mean values of the parasitic components measured from every electrode of the P.W.Circuit Chip. Some values are bounded in order to get a better fit and the software Origin does not give any error in these cases, so these boxes are empty in the table.

Appendix D

First prototype of PCB chip

A first prototype of PCB chip was designed by J.Pinder in order to prove that the problems that appeared in the MIR chip could be solved with this model. The prototype was fabricated using a *High-Z CNC table* machine and a Roger substrate with lower dielectric constant than the silicon used in the MIR chip.

The design of this model is similar to the design of P.W.Circuit chip described in this section, although the gap length could be slightly different in this case due to errors in the fabrication process. Using the pictures of the chip taken with a microscope camera and shown in figure D.1, the length of the gaps could be estimated between 150 µm and 200 µm.

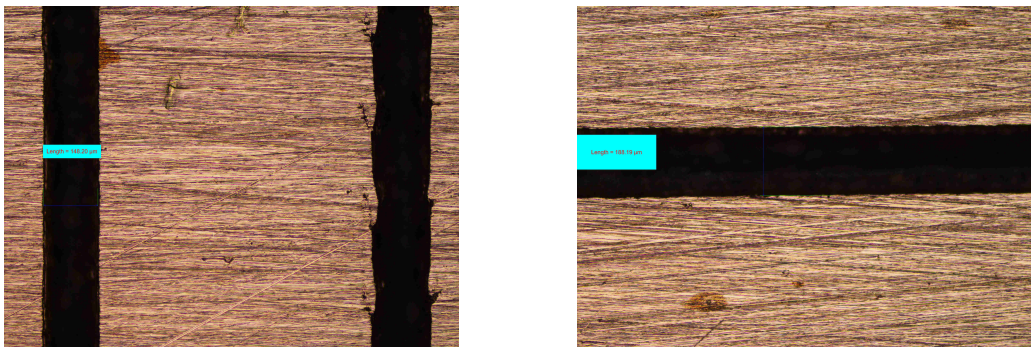

Fig. D.1 Pictures of the gap between the electrodes measured with a microscope camera for the prototype of PCB chip.

The S-parameters are measured by connecting the VNA to the pads of the chip with SMA connectors, crimped to a crimp terminal and attached to the chip with a screw, following the Π network model described in section 4.2.2. This is shown in figure D.2, which is a picture of the set-up for the measurement of the S-parameters from the lower End-cap and lower Correction electrodes, connecting to earth the rest of the chip.

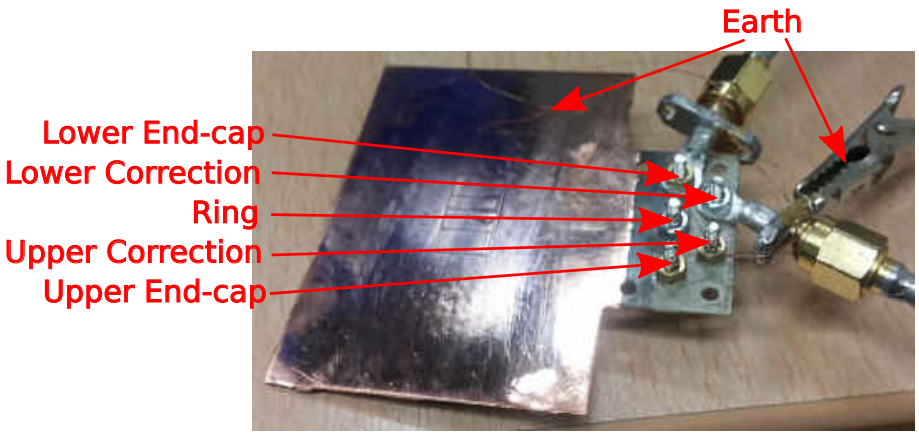

Fig. D.2 Measurement set-up of the prototype PCB chip from the lower End-cap and lower Correction electrodes, grounding the rest of the chip.

It can be observed in figure D.3 that the copper chip is not as symmetric as the wire-bonded chip (results of figure 4.14). It could be due to the difference in the manufacturing techniques, which are more precise in the case of microfabrication. Also, The measurement set-up could be improved, as the connectors are not fixed and it could affect to the measurement. Since it is a prototype and exact results are not required, these details were not perfected, however, the final PCB chip is measured following a different method as described in chapter 4.

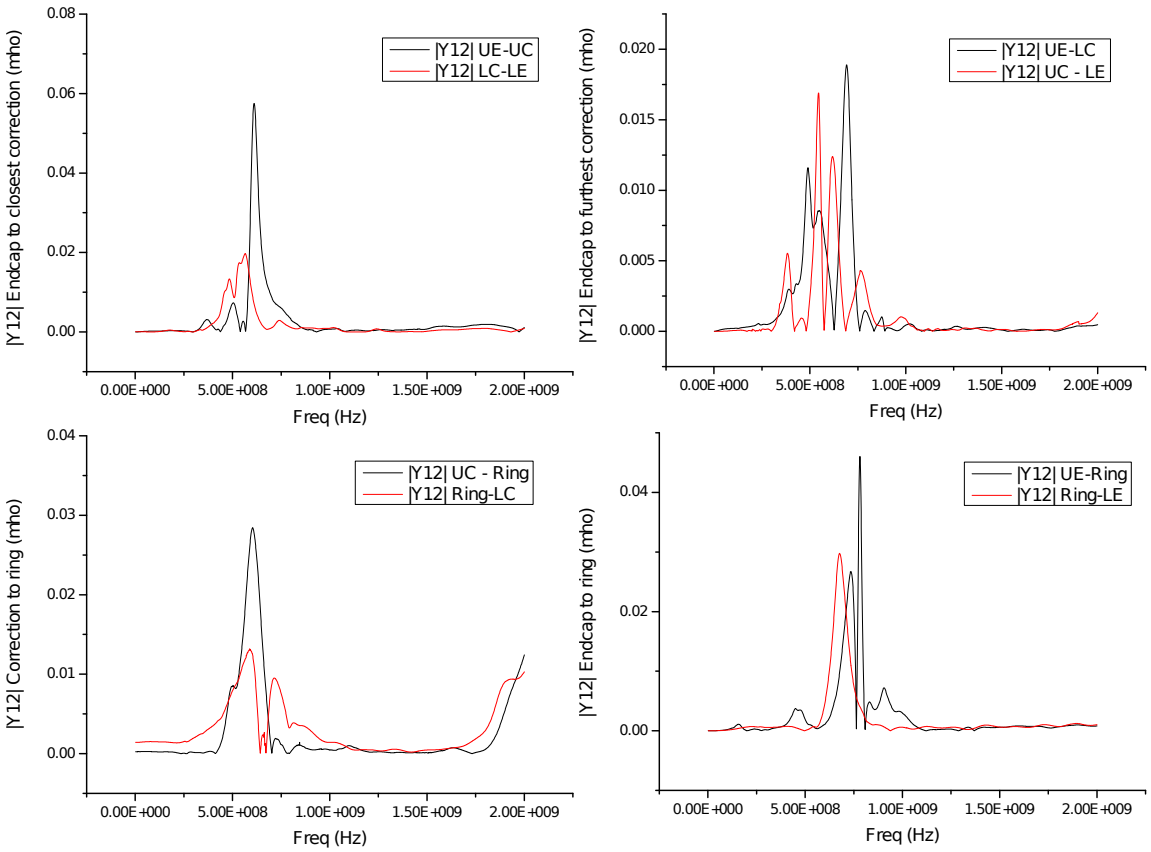

Fig. D.3 Symmetry between the Upper and Lower electrodes in the prototype PCB chip.

The capacitances Y_{in} and $Y_{coupling}$ obtained from the fit of figure D.3 are listed in tables D.1 and D.2. Although there are several resonances in every graph, the data shown in the tables correspond only to the peaks with largest capacitances. They are clearly smaller than the calculated for the wire-bonded MIR chip (tables 4.2 and 4.3). It proves that, by removing the silicon layer on the bottom of the chip, the new design of PCB chip reduces the input and output capacitance, solving the problem of loading the resonator. Additionally, the capacitances between the electrodes are also reduced, since the length of the gap between them is increased, which is another advantage of using this chip. Hence, this prototype behaves as expected and a chip with this design could be used for trapping.

Electrode	Capacitance (pF)	Error (pF)
Upper End-cap	2.06	0.01
Upper Correction	4.22	0.01
Ring	4.60	0.02
Lower Correction	4.89	0.02
Lower End-cap	3.71	0.02

Table D.1 Weighted mean of the input capacitances, obtained from Y_{in}, for every electrode of the prototype PCB chip.

Electrodes	Capacitance (pF)	Error (pF)
End-cap to nearest Correction	1.05	0.01
End-cap to furthest Correction	0.38	0.01
End-cap to Ring	0.80	0.004
Correction to Ring	1.20	0.02
Correction to Correction	1.74	0.005
End-cap to End-cap	0.65	0.02

Table D.2 Weighted mean of the output capacitances, obtained from $Y_{coupling}$, for every electrode of the prototype PCB chip.